INTER-GENERATIONAL COMPATIBILITY STUDY OF MRF EVENT TIMING MODULES

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Abstract

Event timing systems are critical for the synchronization of beam diagnostics and accelerator control at KEK LINAC. Such systems have historically relied on VME-based modules since 2008, such as the MRF 230 series event generator and event receiver. However, with some VME modules approaching their market end-of-life, transitioning to modern platforms like MicroTCA is becoming imperative. This work addresses the challenges of such a migration by focusing on a phased upgrade approach, where new MicroTCA-based MRF 300-series timing modules will coexist with and eventually replace the legacy VME timing modules. A primary concern during this transition is ensuring the functional compatibility between the old and new generations. This paper presents a comprehensive evaluation of critical timing function across coexisting VME and MicroTCA systems. Core compatibility aspects evaluated include event code transmission and reception accuracy, timing precision and jitter, trigger output characteristics, event rate handling, sequencer operation, and timestamp consistency. The findings aim to provide a quantitative assessment of compatibility, identify potential limitations, and offer practical insights for other facilities planning a similar upgrade of their MRF event timing systems, thereby minimizing risk during the accelerator operation.

INTRODUCTION

The KEK LINAC relies on a distributed event-based timing system, which has historically been implemented using VME form factor modules from Micro-Research Finland (MRF) which has demonstrated high stability and reliability in routine operations. However, the VME standard is now approaching obsolescence. In particular, essential components such as the MVME5500 and MVME6100 CPU modules have reached end-of-life and are no longer supported by their manufacturers. At the same time, the MRF 230-series timing modules that form the backbone of the system are being phased out, replaced by the new MRF 300 series available in multiple form factors, including MicroTCA which demands an VME to MicroTCA upgrade.

During the upgrade, legacy and next-generation modules must coexist within the same network, and full functional compatibility must be guaranteed to safeguard accelerator operations. At the same time, the new MicroTCA modules introduce advanced features such as delay compensation, which require careful evaluation in the context of existing operational patterns.

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This paper presents a phased migration strategy for replacing the legacy VME modules with MicroTCA-based MRF 300-series hardware. Particular emphasis is placed on verifying cross-generation compatibility between EVG and EVR modules, assessing performance metrics such as jitter and event transmission accuracy, and developing automated test utilities to streamline large-scale validation. The findings provide both a roadmap for transition and practical insights for other facilities undertaking similar upgrades of event timing systems.

VME TO MicroTCA TRANSITION

Overview of the Current Timing System

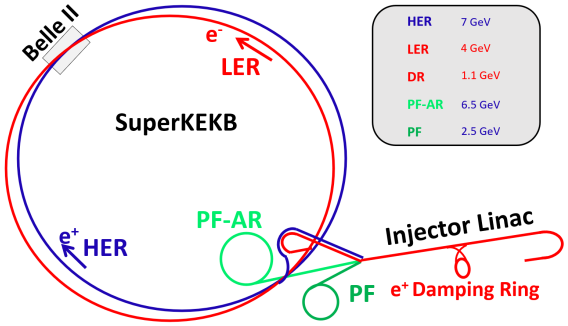

Figure 1: Overview of the KEK LINAC.

As Fig. 1 shows, the LINAC simultaneously provides beam to four storage rings at a repetition rate of 50 Hz. Besides two light sources, PF and PF-AR, the LINAC accelerates electrons to 7 GeV for injection into the SuperKEKB high energy ring (HER). For positrons, the LINAC first injects them into a damping ring (DR) located centrally within the LINAC. After a damping time ranging from 40 ms to 200 ms, the positrons are extracted and continue to be accelerated within the LINAC to 4 GeV before injection into the SuperKEKB low energy ring (LER) [1]. This operational requirement mandates that the timing system delivers stable and reliable synchronization, along with flexible Pulse-to-Pulse Modulation (PPM) operation, to switch the outputs of various accelerator devices every 20 ms [2].

Two operational requirements further constrain the timing system design. First, the trigger sequence must remain phase-locked to the 50 Hz AC mains to stabilize the output from high power kicker magnet power supply used for PF injection. Second, precise RF bucket selection is required across the injector-to-ring chain. While the bucket selection cycle (BSC) for SuperKEKB HER is short (493 µs) and easily accommodated at 50 Hz, inclusion of the positron damping ring enlarges the combined DR–LER BSC to 11.34 ms, complicating AC-phase synchronization [3]. The timing system

therefore applies a sequence shift strategy that preserves AC-locked triggering while maintaining bucket selection for positron injection. Figure 2 shows the diagram of sequence shift. Details related to sequence shift scheme are elaborated in [4].

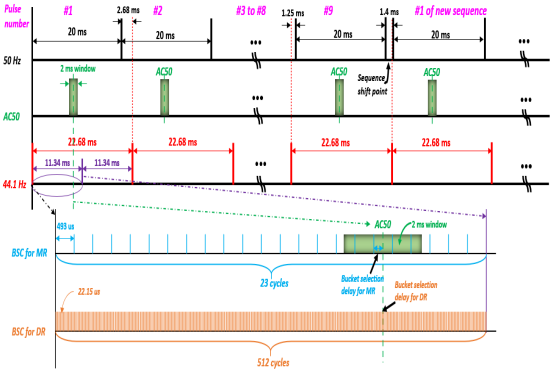

Figure 2: The bucket selection cycle for SuperKEKB DR and MR.

Event Modules

Since 2008, the LINAC utilizes commercial 230 series event generator (EVG) from Micro-Research Finland (MRF) for the timing system. Event receivers (EVRs), connected to the EVG via optical fiber, receive and decode the 8b/10b bit stream to generate triggers for accelerator devices such as klystrons and beam positron monitors (BPM) according to user configurations.

The timing system employed the VME standard, which has demonstrated its stability over decades of operation. The main timing station, serving as the core of the timing system, is responsible for transmitting event codes and data buffers to all EVRs. It utilizes three VME EVG modules to implement the aforementioned PPM and sequence shift functionalities [5].

In practice, the timing infrastructure is diverse, multiple form factors of EVR are selected to specific operational needs. Table 1 shows EVR types used at the LINAC. The majority of EVR stations are implemented in the VME form factor, handling general synchronization and trigger distribution for BPM, klystron and others. The pulsed magnet control system has opted for PXI/PXIe standard to achieve faster bus speeds for data transfer compared to the VME bus. Consequently, 18 PXI EVRs are used to receive trigger signals for the pulsed magnets and to provide high precision timestamp for ADC/DAC waveforms [6, 7].

In addition to the MRF-manufactured EVR products in various form factors, the LINAC also utilizes other EVR solutions. Specifically, to provide bunch-by-bunch triggering signals for the BPMs in the damping ring, modules designated as EVO and EVE, designed from SINAP [8, 9], are installed. Also, for high-resolution RF monitoring, a custom EVR is developed in-house on a Xilinx Virtex-6 FPGA platform, enabling event code decoding and data buffer receiving [10].

Table 1: Diversity of Event Modules

Event generator	Event receiver
VME-EVG-230	VME-EVR-230
VME-EVG-230	VME-EVR-230RF
VME-EVG-230	PXI-EVR-230
VME-EVG-230	SINAP EVO&EVE
VME-EVG-230	Home-made EVR

While this diversity has allowed the timing system to be flexibly adapted to a wide range of applications, it also introduces challenges for future upgrades. The coexistence of VME, PXI, and custom FPGA-based EVRs complicates long-term maintenance and emphasizes the importance of verifying compatibility during the planned transition to MicroTCA-based timing modules.

Features of MicroTCA-based MRF 300 Series

The legacy MRF 230 series is now marked as "no longer available," and MRF's current product line is the 300-series, which covers VME, CompactPCI, PCIe, and MicroTCA form factors. The MicroTCA-based MRF 300 series represents a significant evolution of event timing technology, offering both improved functionality and high performance compared with the legacy 230 series. By leveraging the MicroTCA platform, the system benefits from hot-swappable modules, redundant power and cooling, and standardized high-speed backplane communication. These architectural improvements allow the timing system to be scaled flexibly across a large accelerator facility while reducing maintenance downtime.

From a functional perspective, two new capabilities are particularly important for accelerator applications. The first is delay compensation, which enables precise synchronization of distributed timestamp by calibrating the propagation delays of optical fibers. The second major enhancement is the embedded EVR inside event master (EVM), which integrates the event decoding functionality [11]. The embedded EVR can directly decode postmortem data acquisition events or beam abort events generated from local EVRs and convert it into a system-wide event, which further improves flexibility of the accelerator timing system.

However, these new features also raise the requirements for the planned migration from VME-based MRF 230 modules to MicroTCA-based MRF 300 series hardware. Following the platform transition, the timing system must still preserve AC line phase-locked triggering, maintain event code transmission at 114.24 MHz, and reproduce bucket selection behavior without introducing additional jitter.

Upgrade Strategy

The ultimate goal of the KEK LINAC timing upgrade is to establish a fully non-VME infrastructure that can be sustained in the long term. Achieving this goal requires careful planning to minimize operational risk while progressively introducing new hardware and software components.

The chosen approach is to begin the migration with the EVGs, which form the core of the main timing station, instead of the migration with the EVRs. By removing VME modules from the "heart" of the timing system at an early stage, the upgrade immediately addresses the most critical point of obsolescence and ensures that subsequent improvements build upon a modern, supported platform. Deploying the latest EVG software stack from the outset further strengthens this strategy, since it allows us to take advantage of the advanced functionality of the MRF 300 series from the beginning of the transition.

This phased approach provides two additional benefits. First, it simplifies the later migration of EVRs, which can then be upgraded in a more flexible manner without placing the entire system at risk. Second, it enables incremental system expansion, as new MicroTCA-based EVRs can be introduced alongside legacy units while compatibility is validated. In this way, the timing network can evolve smoothly, maintaining operational reliability while progressively unlocking the advanced features of the 300 series, such as delay compensation and embedded EVR.

By replacing the EVGs first and then gradually phasing out the EVRs, the KEK LINAC timing system can achieve a controlled transition toward a fully MicroTCA-based architecture. This strategy minimizes downtime, safeguards beam operations during the coexistence period, and lays a solid foundation for future scalability and maintainability.

COMPATIBILITY STUDY AND EVALUATION

Experimental Setup

Figure 3 shows the hardware setup of the test bench. The test environment is built on a VadaTech VT814 MicroTCA chassis equipped with a UTC004 MicroTCA Carrier Hub (MCH) and an AMC725 CPU. The timing hardware under study included an MRF MicroTCA-EVM-300 as the EVG and an MRF VME-EVR-230RF as the primary EVR. For compatibility and cross-checks, related modules are also included in the setup: a MicroTCA-EVR-300RF, a PXI-EVR-230 and a VME-EVR-300, enabling direct comparison between different form factors and generations.

Trigger signal measurements are performed using two complementary instruments. A Keysight MXR058A oscilloscope (2.5 GHz bandwidth, 16 GSa/s sampling rate) is used to measure the output waveforms with high precision. In addition, a PicoScope 4424A connected with a Raspberry Pi 5 through USB is actively used. After developing an EPICS driver based on asynPortDriver and creating an IOC on Raspberry Pi, the PicoScope could be remotely controlled through EPICS.

Figure 4 shows the measurement of an EVR output using the PicoScope oscilloscope integrated with EPICS. In this test, the EVR consecutively received three event codes. Each event is configured to generate a 500 microsecond-wide trigger pulse. The captured waveform on the right panel displays three distinct pulses with consistent width and amplitude,

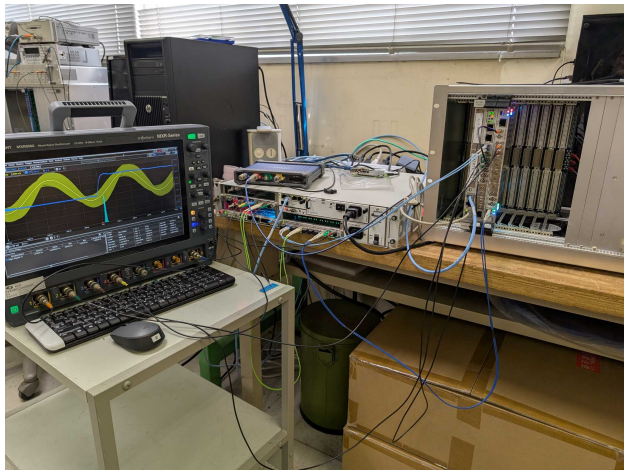

Figure 3: Hardware setup of the test bench.

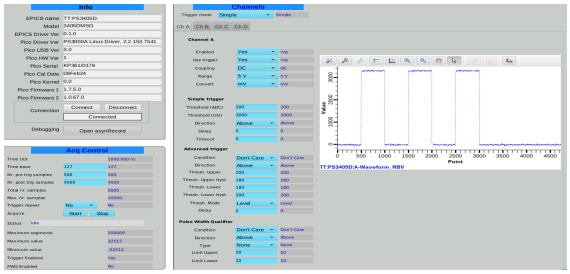

Figure 4: The picoscope captures a waveform from EVR which triggers from sequence of events.

confirming that the EVR correctly responded to each event in sequence.

The CSS-Phoebus OPI on the left demonstrates the configuration of the PicoScope through the custom asynPortDriver-based driver. Parameters such as trigger threshold, coupling, and sampling rate can be set remotely, and the acquired waveform is retrieved directly into the EPICS environment. This setup enabled rapid validation of event-to-trigger mapping and EVR output properties such as trigger polarity and pulse width.

For the software part, the AMC725 CPU is initially shipped with Fedora, but the operating system is reinstalled with AlmaLinux 9 to ensure long-term stability and compatibility with laboratory standards. The control software is based on EPICS 7 together with the mrfioc2 module. To improve compilation efficiency, source trees of both the EPICS base and mrfioc2 are hosted on an NFS server. Because the MicroTCA CPU has relatively poor performance, compilation is carried out on a separate, more powerful server that mounted the same NFS directory.

Furthermore, to provide simultaneous use of MicroTCA and VME hardware during experiments, a unified source tree of mrfioc2 is maintained. This configuration allowed building both Linux executables and VxWorks cross-compiled binaries from the same source. By avoiding redundant compilation steps, this approach speeds up development and simplifys code management, ensuring that modifications to mrfioc2 are consistently applied to both hardware platforms.

Functional Verification

A critical step in the migration process is verifying that the MicroTCA-based EVG-300 modules operate reliably when connected to legacy VME EVR-230 receivers. Since the accelerator environment will inevitably involve mixed generations during the transition, it is essential to ensure that the fundamental functions of the timing system—such as 8b/10b bit stream decoding, configuration register access, and front-panel input/output behavior, remain fully compatible.

To address this requirement, we developed an automated test framework based on the Python pytest library. The framework is designed as a Site Acceptance Test utility capable of replacing manual validation procedures, which are both time consuming and error prone when applied to hundreds of timing modules. The architecture, shown in Fig. 5, integrates Python test scripts running on a Linux server with EPICS IOCs and external measurement devices. Communication with either VME or MicroTCA EVRs and an oscilloscope is handled through EPICS process variables, with the oscilloscope used to capture and verify the precise characteristics of the output pulses.

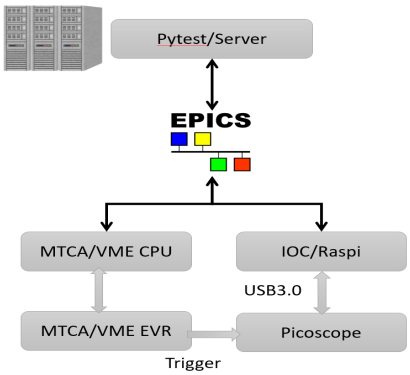

Figure 5: Framework of automated test framework.

The framework adopts an object-oriented design built around three Python classes: a base class for generic IOC communication, and two derived classes for device-specific control of the EVR and oscilloscope. Test cases are organized into modular scripts, covering basic functional checks, front-panel output validation, and interrupt generation from external inputs. Configurability is provided via human-readable YAML files, which define IOC parameters, EPICS protocols, and hardware connections, thereby enabling flexible adaptation to different hardware setups.

Within this framework, basic EVR tests confirmed correct reception and counting of designated event codes, as well as proper operation of heartbeat and status registers. Input/output validation further demonstrated that event codes produced the expected pulse waveforms at the EVR front panel, with pulse width and polarity matching the configured settings. The use of a Picoscope integrated through EPICS allowed precise verification of output signals and confirmed stable behavior across repeated trials.

The results of this functional verification indicate that the MicroTCA-EVG-300 modules are fully compatible with VME-EVR-230 at the fundamental level. All essential functions, including event decoding, register access, and interrupt generation, operated as expected, without anomalies or loss of compatibility. This outcome provides confidence that the phased upgrade can proceed without risk of functional mismatch between the two generations.

Performance Metrics

To assess the timing precision of the mixed-generation system, two types of jitter measurements were carried out: delay jitter and period jitter.

Delay jitter is first evaluated between a MicroTCA-EVG-300 and a VME-EVR-230. In this measurement, the distributed 114.24 MHz event clock is connected to one channel of a Keysight oscilloscope, while the EVR is configured to output a trigger pulse on another channel. The measured delay jitter between the EVR output and the RF reference is found to be 19 ps, as illustrated in Fig. 6. This result demonstrates that the MicroTCA-based generator delivers timing stability that meets the requirements of accelerator operations.

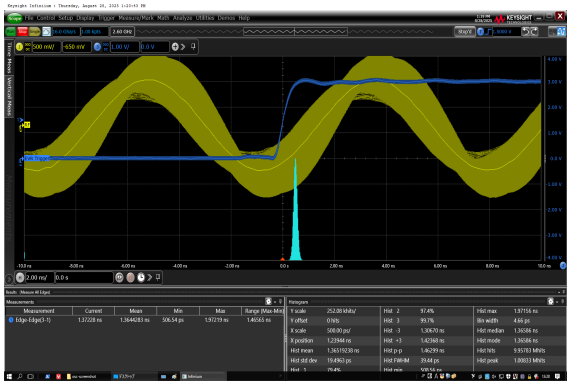

Figure 6: Delay jitter of EVR output.

To further validate cross-generation compatibility, period jitter is measured across multiple EVR configurations. In this test, the oscilloscope simultaneously recorded three output channels corresponding to a PXI-EVR-230, a VME-EVR-230, and a VME-EVR-300. The output frequency is half of event clock which is driven by a MicroTCA-EVG-300. In all three cases, the measured period jitter is approximately 15 ps, indicating that the distribution of the event clock remained consistent regardless of the receiver form factor. For comparison, an additional set of measurements is performed using a VME-EVG-230 as the generator, driving the same three EVRs. The results were indistinguishable, again yielding a period jitter of about 15 ps. Figure 7 shows a representative oscilloscope capture of these measurements.

Taken together, these results confirm that the timing precision of the MicroTCA-EVG-300 is fully compatible with both legacy and current VME and PXI based receivers. The observed jitter performance is consistent across all module

Figure 7: Period jitter measurement from three EVR outputs.

combinations and remains within the low tens of picoseconds, thereby satisfying the SuperKEKB main ring injection requirement.

Long Term Stability

In addition to timing jitter measurements, the interoperability of event code and data buffer transmission between MicroTCA and VME based modules is carefully evaluated. For this purpose, a MicroTCA-EVG-300 is configured to generate event codes and data buffer values, which is subsequently distributed to a VME-EVR-230. A dedicated logging utility based on mrfioc2 is developed to log the received event codes and timestamps which are stored inside EVR internal FIFO [12]. These data are continuously read out and written to disk, while all received data buffer values are similarly saved.

The event code transmission sequence is designed to replicate the injection pattern used in routine KEK LINAC operation. Specifically, the LINAC operates with 12 beam modes, each of which is defined by 11 distinct event codes. A complete beam mode sequence is repeated every 20 ms, and the minimum interval between consecutive event codes is one event clock cycle, corresponding to approximately 8.7 ns at 114.24 MHz. By emulating this operational pattern, the test provides a realistic validation of event delivery under representative accelerator conditions.

The verification procedure employs a Python-based program that automatically compares the transmitted sequence against the EVR log. For each recorded event code, the corresponding timestamp interval is checked to confirm that both the order and timing match the expected pattern. This automated comparison runs continuously, evaluating roughly four million event codes per day. To date, no mismatches have been detected, confirming that the MicroTCA-EVG-300 delivers event codes to the VME-EVR-230 with full accuracy and without timing errors.

A similar validation is performed for data buffer transmission. The contents of the transmitted buffers are retrieved from the EVR and compared against the reference data stream. In all tests performed thus far, no data loss or corruption is observed. These results indicate that both event code transmission and data buffer handling are fully compatible across the MicroTCA-EVG-300 and VME-EVR-230, thereby validating the integrity of this functionality in mixed-generation operation.

CONCLUSION

With the discontinuation of several VME components, a decision has been made to upgrade the VME-based timing system to one utilizing the MicroTCA standard. Given the inherent complexity of the LINAC timing system, a detailed evaluation of inter-generational compatibility is crucial. To this end, we established an experimental setup connecting a MicroTCA-EVM-300 with a VME-EVR-230RF to verify fundamental event link and EVR triggering functionalities. For enhanced detection efficiency, automated testing is performed using a Picoscope and Python scripts based on pytest.

Oscilloscope measurements confirmed that the timing precision and jitter meet the required specifications. To assess long-term stability, we constructed event code patterns based on those used in actual operation and configured the EVG to transmit them to the EVR. The received event codes and timestamps were recorded over several weeks. Comparative analysis against the transmitted patterns revealed no discrepancies, validating the long-term stability of event transmission. Similarly, data buffers were recorded and compared, showing no differences, which further confirms the reliability of long-term data transmission stability.

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