

# Upgrade plan of MicroTCA based event timing system at KEK LINAC

Di WANG

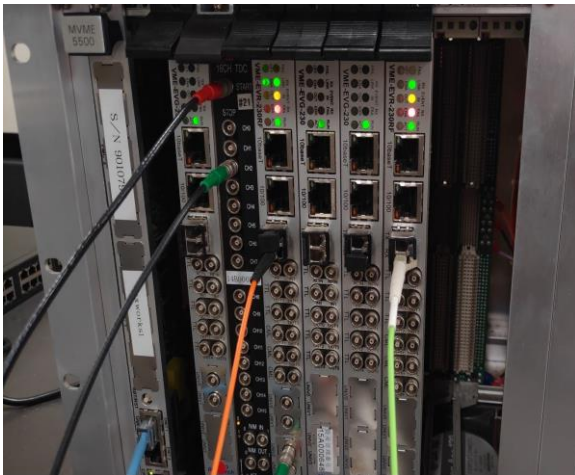
LINAC Control Group

KEK

20250829

# Background: The Timing System Upgrade

- EVG & EVR from MRF company
  - Event Generator (EVG) sends event codes to Event Receivers (EVRs)
  - EVR generates trigger pulse to accelerator devices (BPM, magnet, etc.)
- KEK LINAC relies on a large, distributed timing system with over 100 Event Receivers (EVRs).
- The VME platform is stable but becoming obsolete; key components like the MVME5500/MVME6100 CPU are being discontinued.
- We are migrating our timing system from VME to the modern MicroTCA standard.

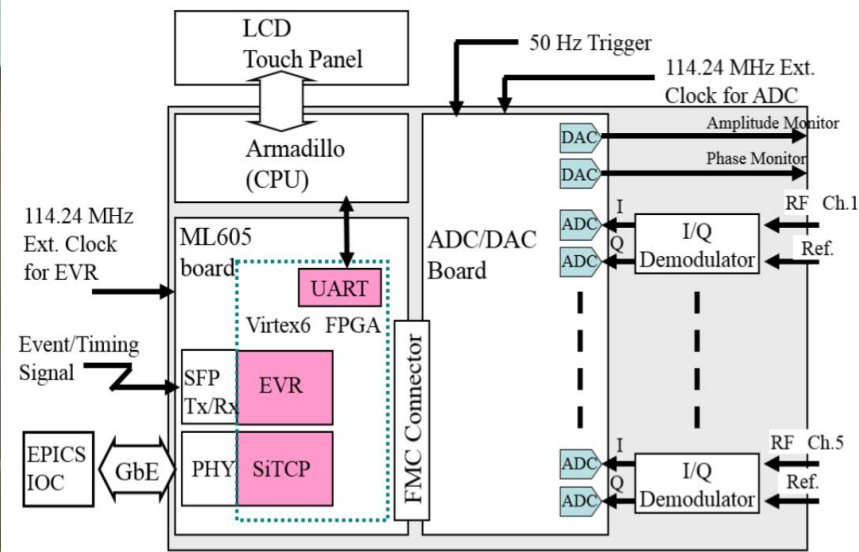
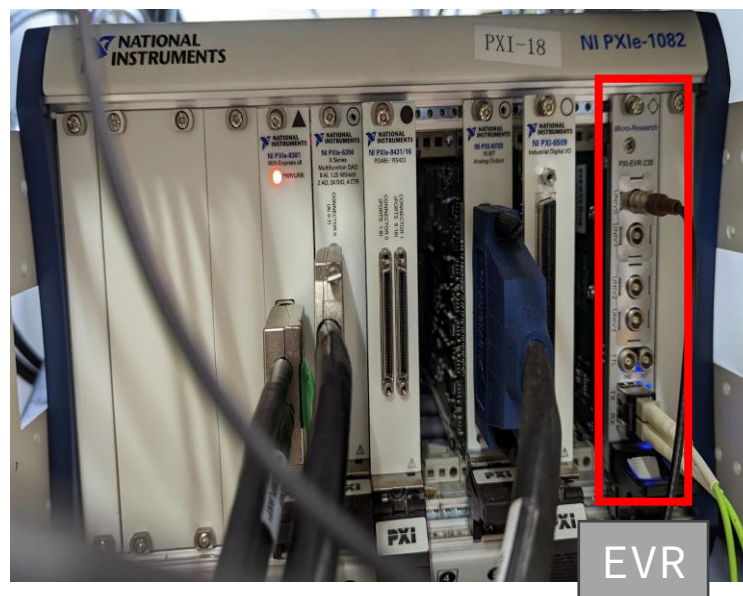


# Considerations Before Upgrade

From	To	Note
VME-EVG-230	VME-EVR-230	In Ope
VME-EVG-230	VME-EVR-230RF	In Ope
VME-EVG-230	PXI-EVR-230	In Ope
VME-EVG-230	Home-made EVR	In Ope
VME-EVG-230	MTCA-EVR-300RF	??
VME-EVG-230	MTCA-EVR-300U	??
VME-EVG-230	VME-EVR-300	??
MTCA-EVG-300	MTCA-EVR-300U	○
MTCA-EVG-300	MTCA-EVR-300RF	○
MTCA-EVG-300	VME-EVR-300	○
MTCA-EVG-300	VME-EVR-230RF	??
MTCA-EVG-300	VME-EVR-230	??
MTCA-EVG-300	PXI-EVR-230	??
MTCA-EVG-300	Home-made EVR	??

Combination table of EVG and EVR

- Various EVR types are used
  - PXI-EVR-230 for pulsed magnet control
  - Home-made EVR (Virtex6 FPGA) for RF monitor
  - SINAP EVR
- We need to consider
  - Compatibility between timing module generations
  - Compatibility among various form factors



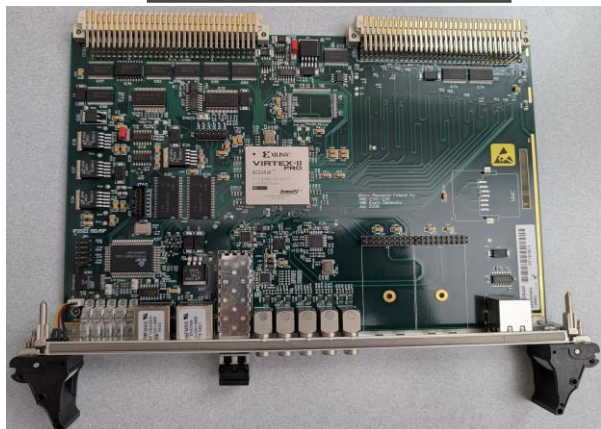
# What MicroTCA + MRF 300 Series Offers

- **VME**
  - **Proven stable:** has been proved reliably in accelerator environments
  - **Long lifecycle:** has been running for decades
  - **EPICS integration:** tightly coupled with mainstream control systems framework - EPICS
- **MicroTCA**
  - **Modern, Stable:** redundant design (MCH, PM, CU) for high stability
  - **Long-term support:** with an active market
  - **System management:** health monitoring, alarm and remote diagnostics via MCH/IPMI
  - **High bandwidth backplane:** Support high-speed data acquisition
  - **Hot-swap feature:** maintainability
- **MRF 230 Series**
  - **Trigger events:** distribution of event codes on a stimulus
  - **Sequencers:** support for complex, pre-programmed event sequences
  - **Timestamp distribution logic:** provides global timestamp for synchronized data acquisition
  - **AC line synchronization:** locked to mains cycle for periodic operations (50/60 Hz)
  - **EPICS IOC integration:** mature EPICS drivers (mrfioc2) and database support, widely deployed
- **MRF 300 Series**
  - **Delay compensation:** compensate transmission delay
  - **Flip-Flot output:** Pulse generator X for set, X+1 for reset. Interlock logic possible
  - **Embedded EVR:** upstream event link, suitable for post-mortem analysis



# Two Migration Strategy

VME EVG 230



MTCA EVR 300



Path A: **Replace EVRs first**

MTCA EVG 300



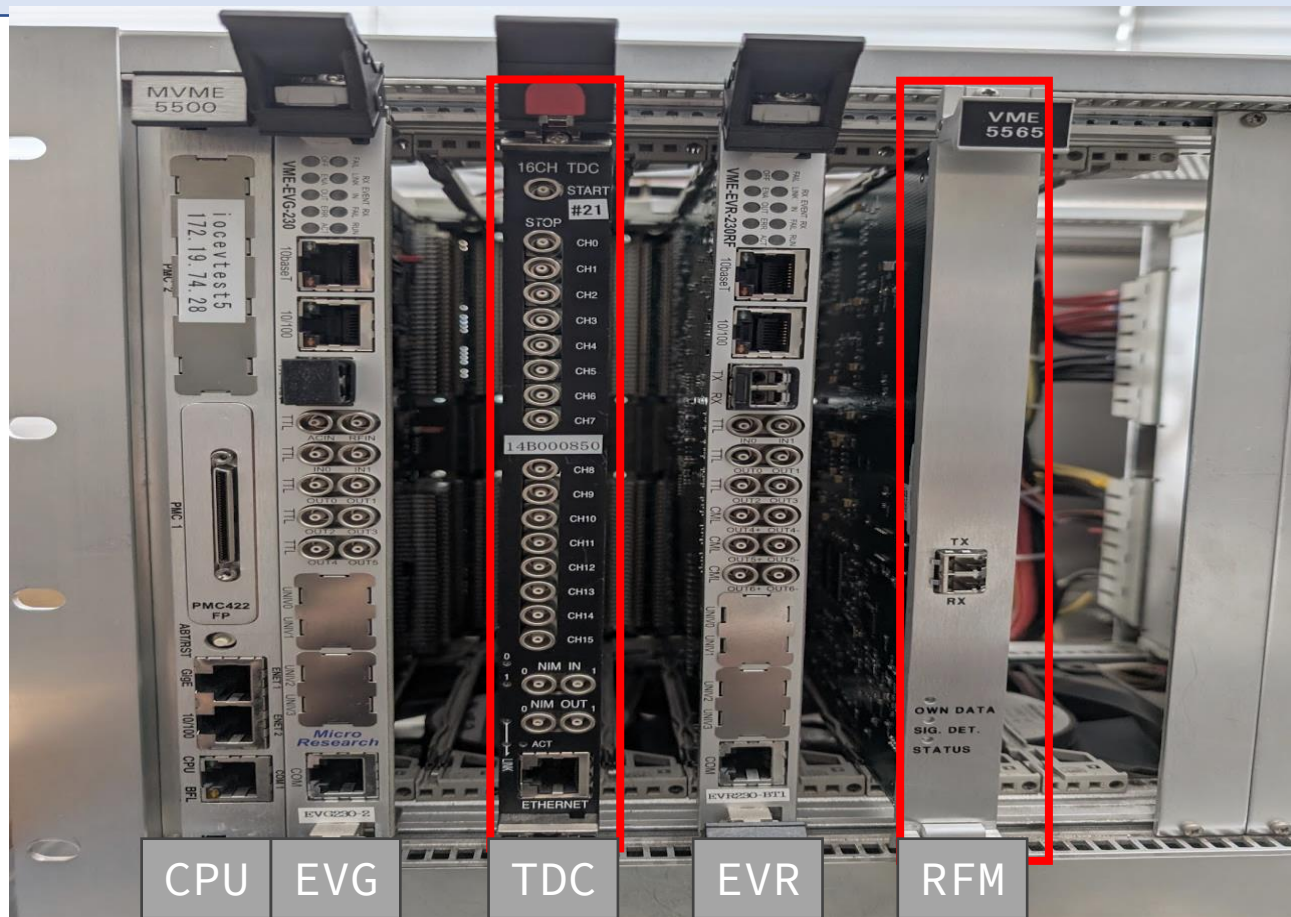
VME EVR 230



Path B: **Replace EVG first**

- Ultimate goal: fully non-VME timing system
- Chosen approach: **replace EVG first**
  - Remove VME from the “heart” of the timing system
  - Deploy the latest EVG software stack from the start
  - Unlock advanced functionality of the MRF 300 series
  - Simplify subsequent EVR migration and system expansion

# Other Considerations Before Upgrade

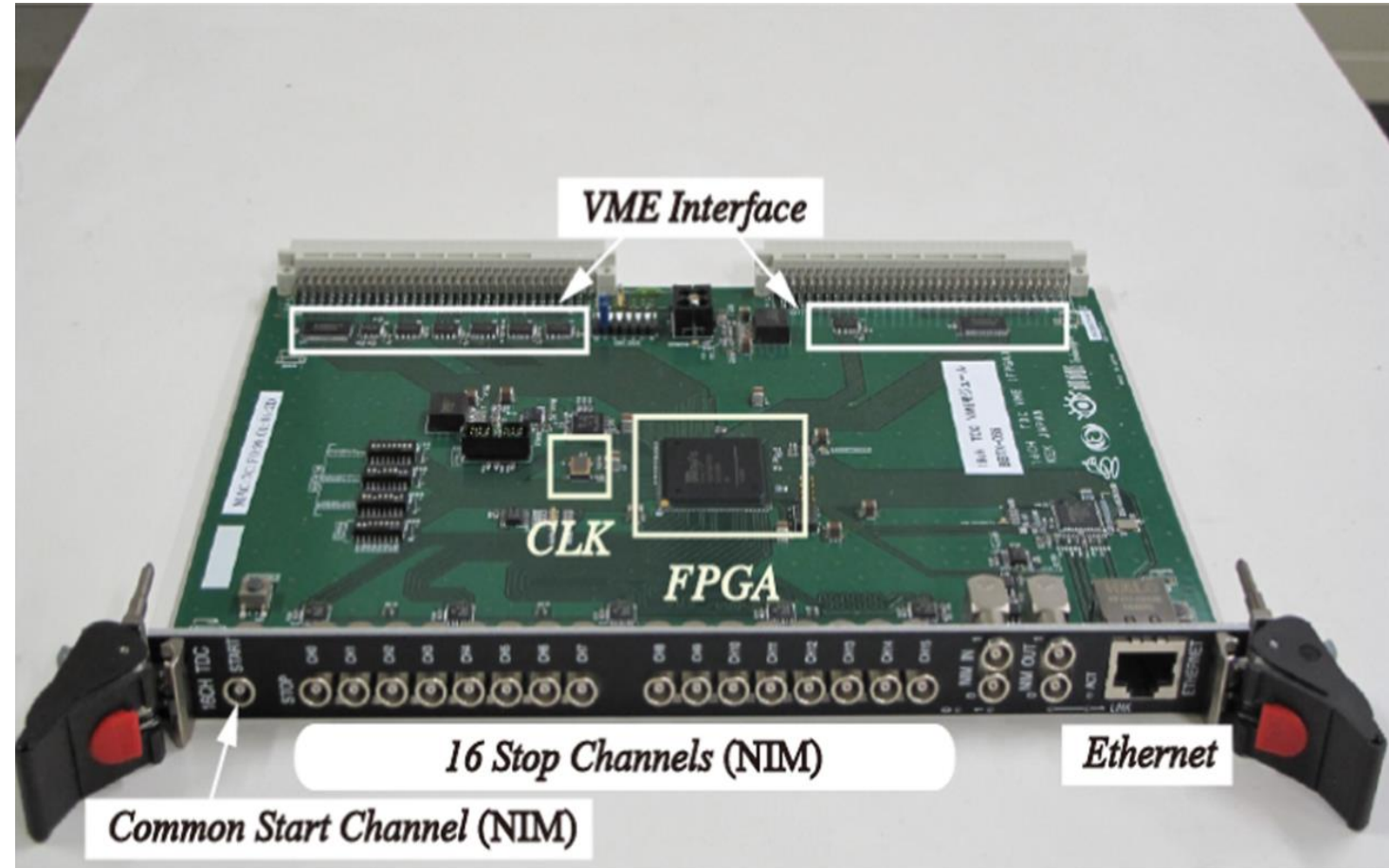


- Besides of MRF timing modules, timing system also use auxiliary VME modules
- Home-made TDC (Time-to-digital Converter)
- Reflective memory (VME-5565) from Abaco



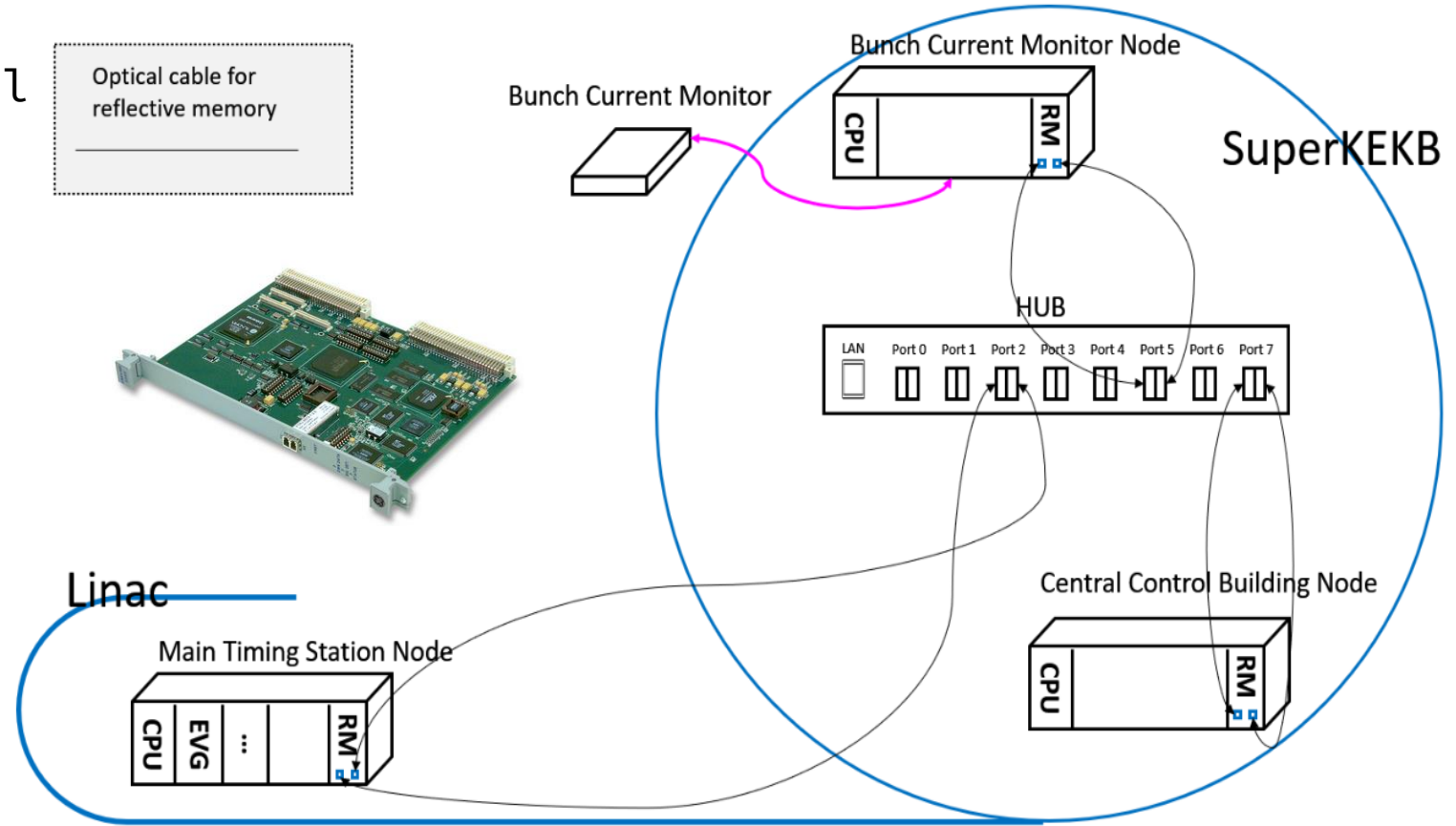
# Other Considerations Before Upgrade

- 16 channel
- 32 bit counter with 1 ns resolution
- Usage
  - For EVG: Measure phase of AC line and synchronize events with AC line
  - For EVR: Measure and log EVR trigger delay for diagnosis
- Need to develop (or purchase?) TDC module of AMC form factor



# Other Considerations Before Upgrade

- Fiber-optic connected nodes
- data written into SDRAM of local nodes is broadcasted to other nodes
- Bunch current monitor in SuperKEKB ring share data with bucket selection node.
- Bucket selection node decide next injection bucket
- Main timing station node apply the change
- Vendor provides RFM of 3 form factor: VME, PCIe, PMC
- AMC carrier for PMC is needed
  - COTS from N.A.T. and VadaTech is available

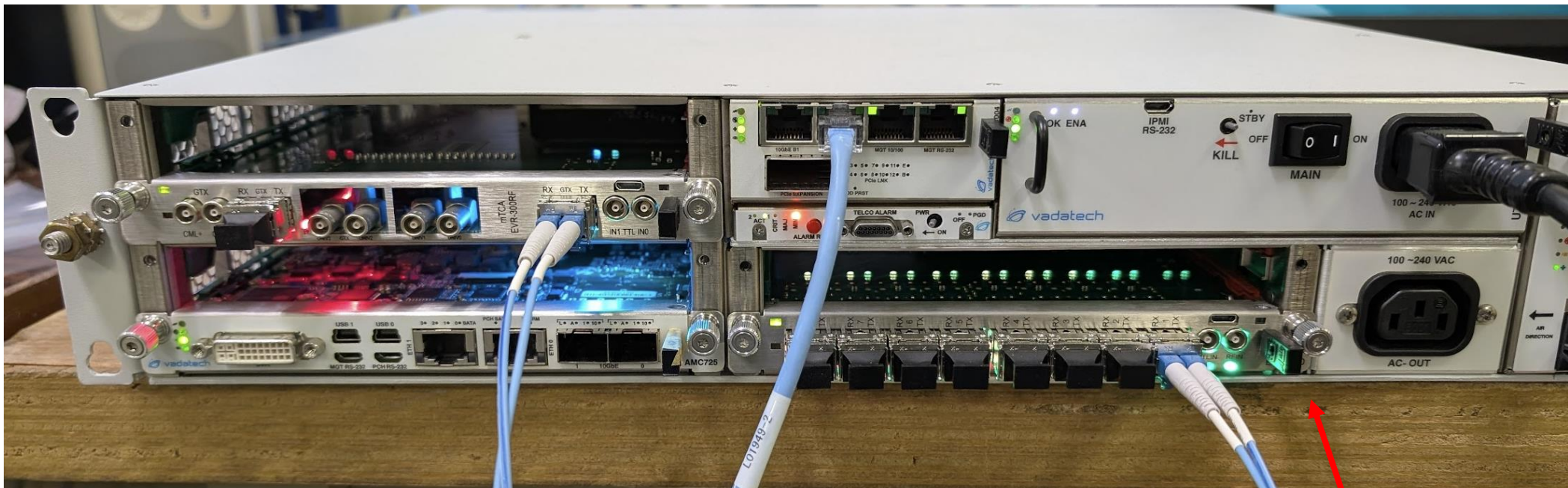




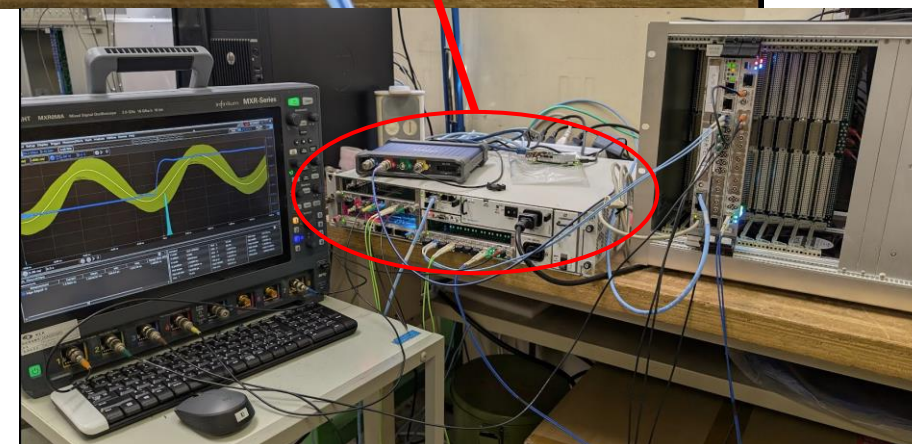
# Phased Upgrade Plan

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- Phase 0 – Test & Validation ← WE ARE STILL HERE!
  - Install MTCA-EVG-300 + VME-EVR-230 in a lab or test stand
  - Verify event stream compatibility with VME modules
  - Validate EPICS IOC support, monitoring, and operator interface
  - Run long-term stability tests before touching production
  - Keep software continuity
- Phase 1 – Deploy MTCA EVG
  - Replace VME EVG with  $\mu$ TCA EVG in the production system
  - Fallback to legacy EVG if unexpected issues arise
- Phase 2 – Mixed Environment
  - Gradually phase out VME EVRs at selected devices
  - Operate in mixed mode (MTCA-EVG-300  $\rightarrow$  VME-EVR-230 + MTCA-EVR-300)
- Phase 3 – Full Migration
  - Replace all remaining VME EVRs with MTCA EVRs
  - Activate more advanced MTCA features



- VadaTech Chassis: VT814
- VadaTech MCH: UTC004
- VadaTech CPU: AMC725
  - Preinstalled Fedora OS & reinstall AlmaLinux 9
  - EPICS 7 & mrfioc2 (EPICS module) on NFS
- MRF MTCA-EVM-300
- MRF MTCA-EVR-300RF, VME-EVR-230RF, VME-EVR-300



# Early Results



SuperKEKB MR Requirement: <30 ps



Front panel can only output half of event clock, which is  $114 \text{ MHz}/2 = 57 \text{ MHz}$   
 EVR can output 114 MHz on backplane  
 TCLKA/B



## TT:VME-EVR-230 Expert

Global		Status		Event Monitors	
Enable	Enabled	Enabled	Enabled	@OBJ=EVR230RF,Code=	153940
Requested Freq	114.240 MHz	Link Status	OK	@OBJ=EVR230RF,Code=	0
Actual Freq	114.240 MHz	PLL Status	OK	@OBJ=EVR230RF,Code=	0
Clk Err	0.000 KHz	Time Status	Valid	@OBJ=EVR230RF,Code=	0
Ext Inhib (GTX only)	Use Inhibit	Link Err Cnt	1	@OBJ=EVR230RF,Code=	0
	THU, 28 AUG 2025 13:13:54	HBt TIMO Cnt	1	@OBJ=EVR230RF,Code=	0
Clock Mode	EVG	Fw Version	006.0	@OBJ=EVR230RF,Code=	0
Time Src	Event clock	Sw Version	2.7.2	@OBJ=EVR230RF,Code=	0
Time Clk	114.240 MHz	HW Model	VME-EVRRF-230	@OBJ=EVR230RF,Code=	0
Time Clk Div	1	Position	Slot #4	@OBJ=EVR230RF,Code=	0
Link RX Mode	DBus+Buffer	IRQ Rate	2 Hz		
Link TX Mode	DBus+Buffer	FIFO Rate	2 evt/s		
		FIFO Loop Rate	2 Hz		
		Evt Avg of FIFO	0.196 %		
		Commit Hash	NotConfi		

SFP	
SCAN	10
Rx Pwr	497.5 uW
Tx Pwr	404.2 uW
Temperatu	27.2 C
Link	4300 Mb/s
Vendor	AVAGO
Part	AFBR-57R5
Serial #	A90752HP
Manu.	2007/12

Mappings	
Blink Evt 1	125
Blink Evt 2	0
PS Reset	123

OPI VME-EVR-230

## TT:MTCA-EVR-300 Expert

Global		Status		Event Monitors	
Enable	Enabled	Enabled	Enabled	@OBJ=EVR,Code=10	154124
Requested Freq	114.240 MHz	Link Status	OK	@OBJ=EVR,Code=11	0
Actual Freq	114.240 MHz	PLL Status	OK	@OBJ=EVR,Code=12	0
Clk Err	0.000 KHz	Time Status	Valid	@OBJ=EVR,Code=13	0
Ext Inhib (GTX only)	Use Inhibit	Link Err Cnt	1	@OBJ=EVR,Code=14	0
	Thu, 28 Aug 2025 13:14:31 +0900	HBt TIMO Cnt	3	@OBJ=EVR,Code=15	0
Clock Mode	EVG	Fw Version	207.20	@OBJ=EVR,Code=16	0
Time Src	Event clock	Sw Version	2.7.2	@OBJ=EVR,Code=17	0
Time Clk	114.240 MHz	HW Model	mTCA-EVR-300RF		
Time Clk Div	1	Position	9:0.0 slot=2		
Link RX Mode	DBus+Buffer	IRQ Rate	2 Hz		
Link TX Mode	DBus+Buffer	FIFO Rate	2 evt/s		
		FIFO Loop Rate	2 Hz		
		Evt Avg of FIFO	0.196 %		
		Commit Hash	NotConfi		

SFP	
SCAN	10
Rx Pwr	738.3 uW
Tx Pwr	656.1 uW
Temperatu	36.2 C
Link	10300 Mb/s
Vendor	FS
Part	SFP-10GSR
Serial #	G23301263
Manu.	2023/08

Mappings	
Blink Evt 1	125
Blink Evt 2	0
PS Reset	123

Delay Compensation		Software Event	
Enable	Enable	Send Event	0
Target	1000.000 r	TS Tx	Disabl
Status	Locked	Time Err	-1
Actual	151.311 n	TS	Sun, 07 Feb 2106 1
Correction	848.687 n		
Loop Trk	Lock		
Master Rx	Fine		
ID	0x5		

OPI for MTCA-EVR-300

Keep EPICS PV name and OPI consistency for various of form factors



- Upgrade plan defined
  - Goal is a fully non-VME timing system with MTCA + MRF 300 modules
  - Phased migration approach ensures safety and compatibility
- Compatibility validated
  - Event code distribution tested and confirmed functional
  - Jitter performance within requirements – no degradation observed
- Next migration tasks
  - Replace remaining VME-based timing modules (TDC/RFM) with MTCA versions
  - Develop new Linux driver for MTCA TDC/RFM modules
  - Integrate into EPICS and conduct system-level tests
- Final target
  - A robust, maintainable, and future-proof MTCA timing system
  - Smooth transition for operators with improved monitoring and reliability