DIGITAL CONTROL SYSTEM FOR SOLID STATE DIRECT DRIVE® RF-LINACS

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Abstract

The Solid State Direct Drive® concept for RF linacs has previously been introduced[1]. Due to the different methodology (i.e. solid state based rather than electron tube based) as compared with conventional RF sources a new control system is required to deliver the required LLRF. To support this new technology, a fully digital control system for this new concept has been developed. Progress in digital – analog converter technology and FPGA technology allows us to create a digital system which works in the 150 MHz baseband. The complete functionality was implemented in a Virtex 6 FPGA. Dispensing the PLL allows an excellent jitter-behaviour. For this job, we use three 12 bit ADCs with a sampling rate of 1 GS/s and two 16 bit DACs (1 GS/s). The amplitude of the RF source is controlled by dividing the RF modules mounted on the power combiner[2] into two groups and controlling the relative phase of each group (in effect mimicking an "out-phasing" amplifier). This allows the modules to be operated at their optimum working point and allows a linear amplitude behaviour.

CONCEPT

The availability of fast components (ADCs DACs) and the progress in FPGA-technology offers a new view on the LLRF-loop. Pickup signals can be converted to digital directly without down conversion. The computing can be realised by massive parallel structures in the FPGA and the digital output signal does not have to be up converted. A distributed control-system structure offers a scalable flat design. For the F-class-amplifier requirement we choose an out phasing architecture which allows to vary the power inserted into the cavity without modification of the amplitude.This is illustrated in Fig. 1.

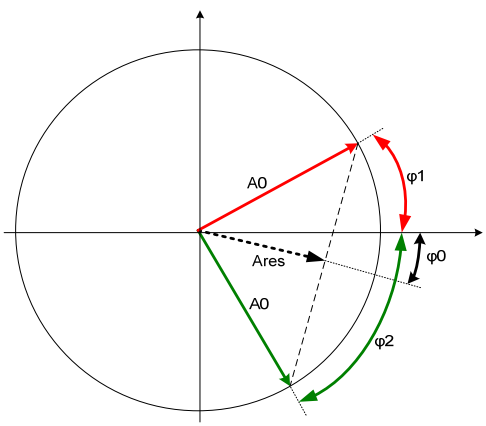

Figure 1: Principle of out phasing control.

Two groups of RF-Modules are driven separately with φ1 and φ2. The cavity-gap works like a combiner and inserts only the vector-summation Ares and φ0. A special filter design in the output network prevents power loss in inversely phased vector components. Phase-modification can be realised by tilting the angles of both RF-module-vectors (φ0).

$$\varphi 0 = \frac{\varphi 1 + \varphi 2}{2} \qquad Ares = A0 * \cos\left(\frac{\varphi 1 - \varphi 2}{2}\right)$$

One of our primary requirements was to design a scalable system. Thus, all physical units have to be built with their own subsystem hiding avoidable problems to the upper system layer. The idea was to handle controls and problems as near as possible to the source. For example, the control computer (CC) tells the subsystem controller cavity (SCC) only field strength, pulse length, phase and the timestamps. CC doesn't need the inner knowledge about how real components work (number of RF-modules, used power supply) in the subsystem. SCC handles its part of work by itself or, if execution violates possible working area, reports the problem to the CC.

Figure 2 shows the concept:

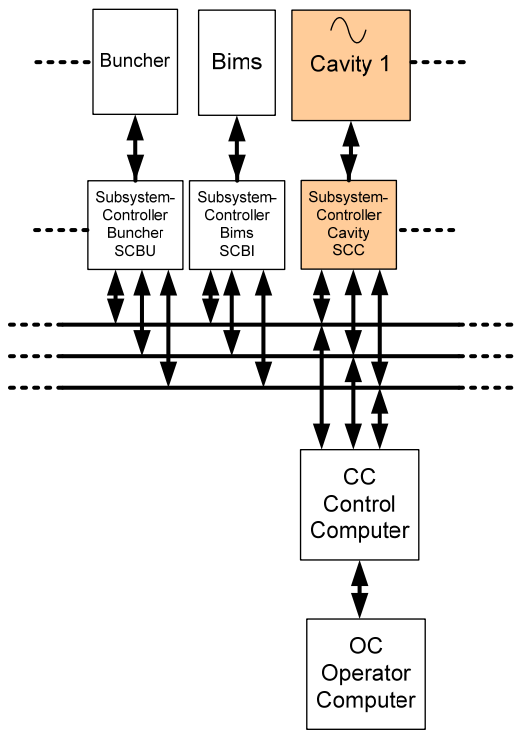

Figure 2: Concept of distributed control system.

This way, system-level complexity will be minimised and because of encapsulating, the choice of subsystems is easier. In first step we are focused on creating a prototype of control system for our High Voltage Test Rig (HVTR)[1] experiment. Figure 3 shows the structure of the SCC. The Sub controller-cavity-communication (SCCC) is managing all upper controls like GPIB, RS485 etc which are not realtime. It's also the communication-interface for the subcontroller cavity realtime (SCCRT). The SCCC is realised by a National Instruments™ PXI-rack. This choice provides a very easy adaptation of measurement-components to our system.

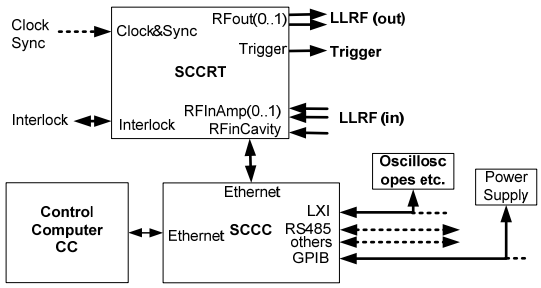

Figure 3: Structure of SC.C

The SCCRT controls all time-critical components in the cavity system. The major focus was to design a full digital signal path for the LLRF. Taking care of design risks we choose a multi PCB-Solution for the first step shown in Fig. 4.

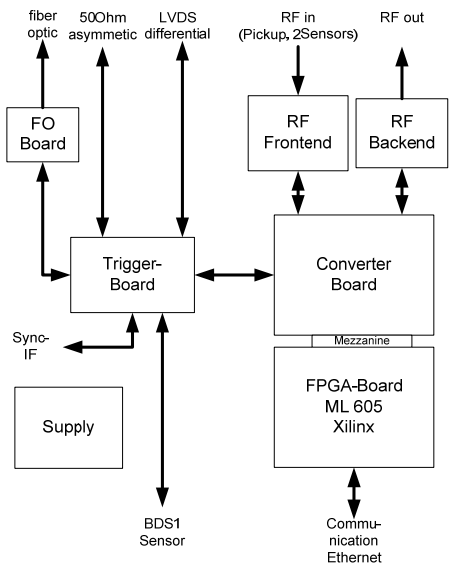

Figure 4: Topology of SCCRT.

To handle the immense amount of data, the FPGA has to serve massive parallel information-streams as shown in Fig. 5.

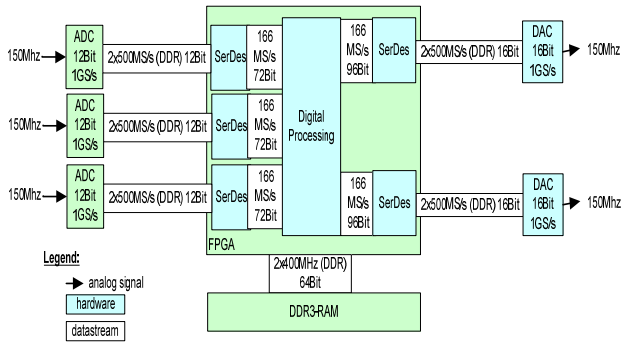

Figure 5: Dataflow on SCCRT.

Each ADC generates a data-amount of 1GS/s, which is streamed in DDR#-Technology with 2x500MS/s each. These streams are "flattened" by SERDES+ structures in the FPGA to 166MS/s with a bus width of 72Bit. The digital processing works with massive parallel computation.

On the output side, we created two 166MS/s 96Bit width busses to get full functionality of DAC. They will be fed by 2x500MS/s with a resolution of 16Bit.

Currently we are preparing our first experiment to load the RAM of the SCCRT with predefined signal shapes and make a controlled "shot" to the HVTR-cavity. The timing core will also be tested in this step. This core enforces us to create a 1ns timing grid to control all components and prepare future synchronisation-functionality.

REALISATION

The controlling software is realised in LabView™ with object oriented driver interface.

Here are some views on our first device. The SCCRT is mechanically mounted on a 19"-Rack. Front plate (Fig. 6) looks puritan caused by the idea, hosting all permanent connections on the backside (Fig. 7). Only connections for monitoring, serving and safety are on the front plate.

Figure 6: Front plate of SCCRT.

*HVTR was the first λ/2-resonant cavity driven with solid state technology. Therewith we made the proof of concept in 2010.

The backplane provides the plugs to all needed devices.

Figure 7: Backplane of SCCRT.

Fig. 8 is showing the open SCCRT. On the right side (base layer), you can see the FPGA-board, in the middle the converter-board (2nd fan) and in the left the trigger-board. On the upper layer there are the RF-frontend boards.

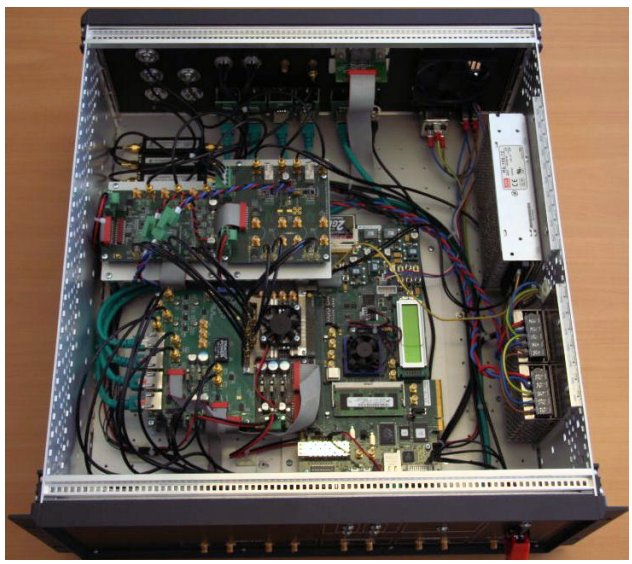

Figure 8: Topology of SCCRT.

FIRST RUN

On the first run of the SCCRT we got problems with the RF-filter-design, but after some patches the signal-quality seems good enough to start experiments with the HVTR. Fig. 9 demonstrates a sinus output with 166Mhz. Channel 1 and Channel 2 represents both DAC-channel outputs, Channel 3 and 4 are the resulting signals on outputs.

Currently we are working on a redesign of the RF-frontend-/and -backend-PCBs to optimise the RF performance and on optimising timing constraints on the FPGA-core.

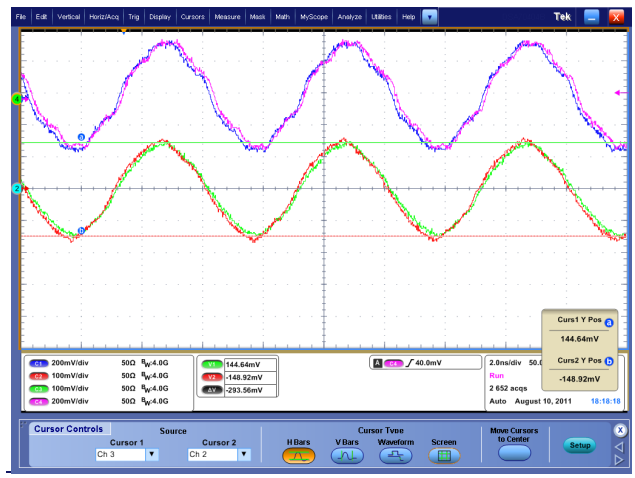

Figure 9: Signals on LLRF output.

FUTURE WORK

- HVTR-Cavity experiment with predefined pulse shapes to verify built hardware and software.
- Analysing HVTR-stability mechanism and behaviour. Influence of capacitor-bank, thermal effects on transistors and compensation-strategies.
- Create an IP-core for macro pulse regulation.
- Redesign of SCCRT for next implementation step. Exploration of 3M ECM™-prepreg[3].

REFERENCES

[1] O. Heid, T. Hughes, Proc. of IPAC10, THPD002, p. 4278, Kyoto, Japan (2010).
[2] O. Heid, T. Hughes, Proc. of LINAC10, THPD068, Tsukuba, Japan. (2010).
[3] Product of 3M™ http://www.3Mcapacitance.com

DDR Double Data Rate (rising and falling edge of clock flags separate data words.