

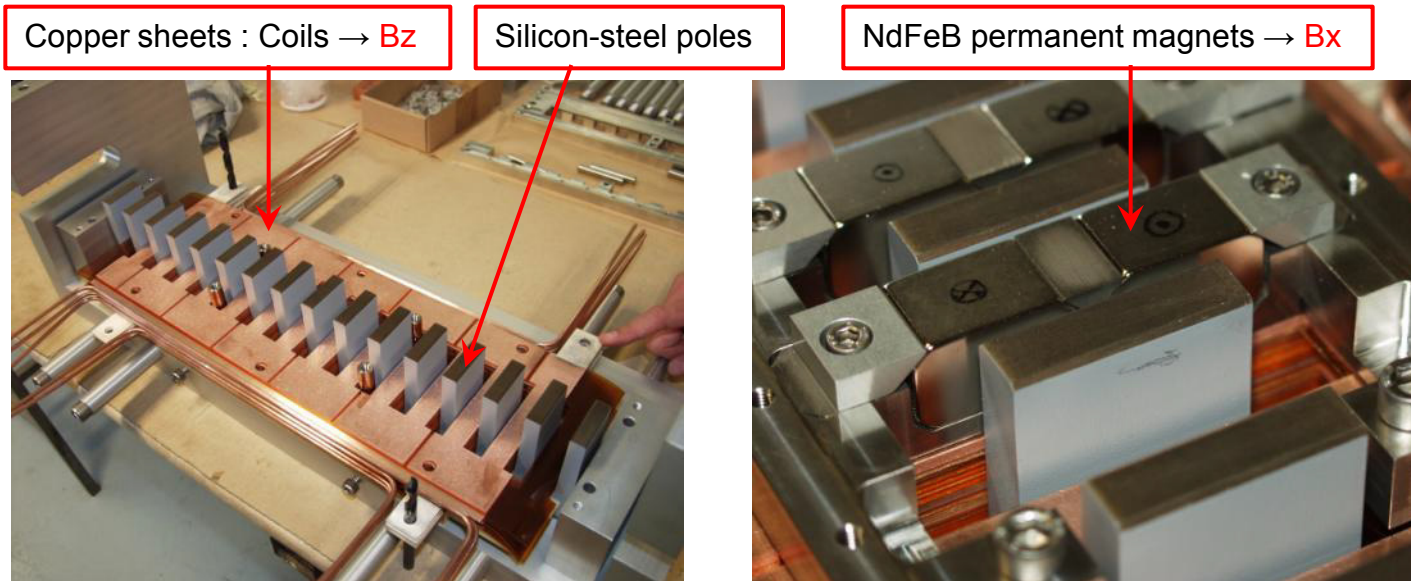
Innovative Design of the Fast Switching Power Supplies for the SOLEIL EMPHU Insertion and its Fast Correctors

F. BOUVET

On Behalf of the SOLEIL Power Supply Team

- **Context of the project**
- **Power supply requirements**
- **Main power supply design**
 - Topology
 - Power converter sizing
 - Digital control loops
 - Dynamic performances
 - Influence of the real load behavior
- **Corrector power supplies**
 - Design
 - Power supply driving
- **ID Feedforward compensation**
- **Questions**

- A new electromagnetic/permanent helical undulator, with a 65 mm magnetic period, is under development at SOLEIL
- This insertion device should provide a fast switching ($< 100\text{ms}$) of the photon polarization to perform dichroism experiments
- **Design of the undulator *** :



$$B_x = B_z \\ = 0,24 \text{ T}$$

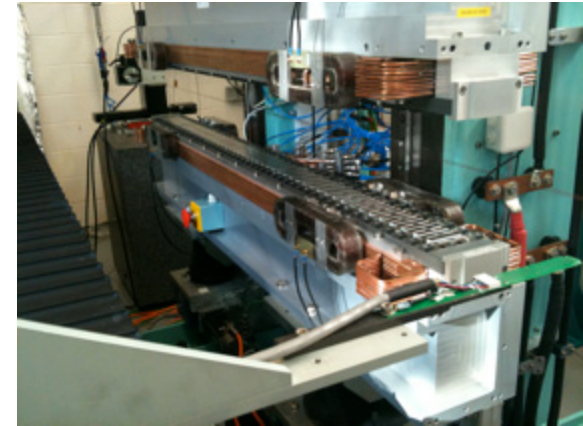
* F. Marteau, "Development of an Electromagnetic/Permanent Helical Undulator for Fast Polarisation Switching", PAC'09

Designed undulator

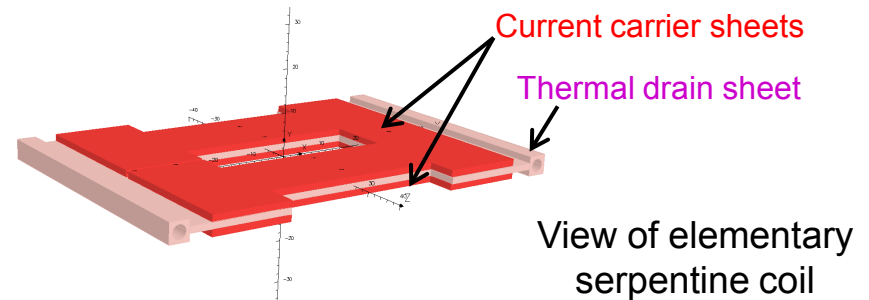
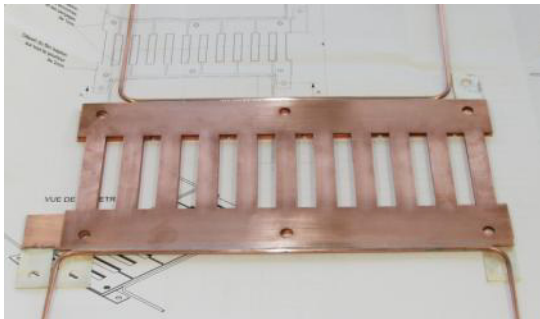
- Prototype (SEF)



The prototype is fixed on 2 girders attached to a motorized carriage → Vertical movement to change peak field values



- **Coil cooling:** Use of thermal drain sheets cooled by tubing brazed to their outside edges
1 thermal drain sheet for every 2 current carrier sheets → Every conductor has one surface in contact with a cooling plate (through insulation)



- **Main power supply:**

- Feeding the coils producing the vertical field:
 $R = 130 \text{ m}\Omega$; $L = 4 \text{ mH}$ to 8 mH depending on the delivered current
- 4-quadrant operation
- Maximum current $\pm 350 \text{ A}$
- Polarity switching time $< 50 \text{ ms}$
- Current precision: 100 ppm of the nominal current
- Current reference: Trapezoïdal shape with rounded corners.
Repetition rate will extend between DC and 5 Hz

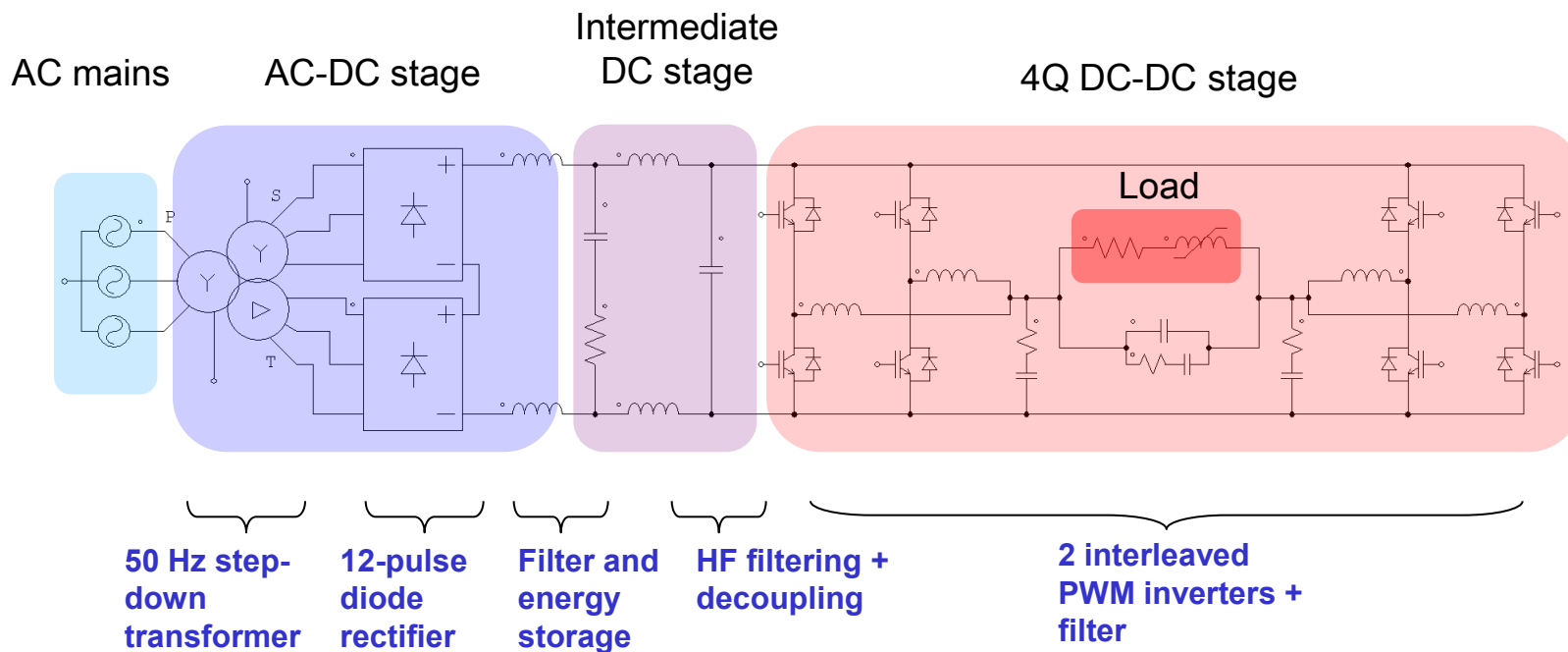
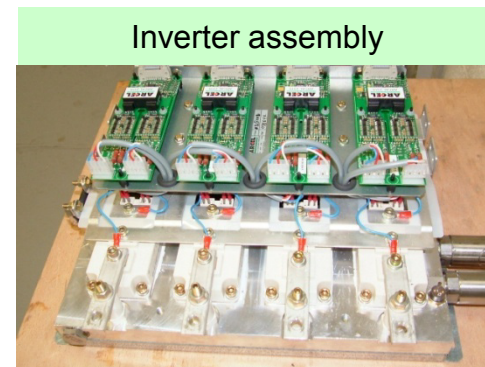
- **8 Corrector power supplies:**

- Feeding the correction coils used to compensate any beam closed orbit distortion consecutive to main field transitions
- Rated between $10 \text{ A} / 100 \text{ W}$ and $20 \text{ A} / 200 \text{ W}$
- Should provide at least as fast response as the main PS
and should be **synchronised with it** ($< 1 \text{ ms}$)

Main power supply design

- Structure of the converter:**

12-pulse rectifying unit + filter and energy storage
+ 2 interleaved PWM inverters + filter



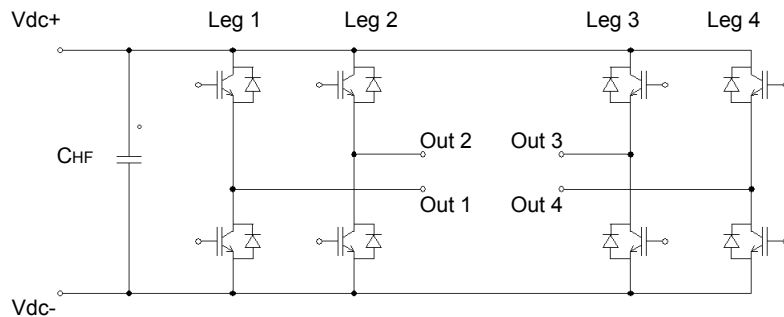
Rather simple structure: Favours reliability and eases up maintenance

- This topology choice is linked to the following considerations:
 - ❑ AC-DC stage:
 - Requirements: Galvanic isolation between mains and output load + adjustment of the DC link voltage level
 - Chosen solution: 50 Hz transformer + 12-pulse rectifier
 - Well-known and reliable solution
 - DC link voltage predominating harmonic theoretically at 600 Hz (easy to filter)
 - No additional power switches have to be controlled other than the ones used in the 4Q DC-DC stage: The whole converter can be controlled using a single SLS digital control unit
→ Increased reliability + reduced costs
 - ❑ Intermediate DC stage:
 - Formed by a slightly damped LC filter
 - Used to attenuate the harmonics produced by the 12-pulse rectification and to mitigate the impact of AC mains perturbations
 - When the load acts as a generator, the energy is transferred to the capacitor bank (energy storage)

Main power supply design

❑ 4Q DC-DC stage:

- The inverter section consists of 2 interleaved PWM H-bridges
- Chosen interleaved PWM control strategy: 180° phase shift between leg 1 and leg 2 and between leg 3 and leg 4 + 90° phase shift between legs 1, 2 and legs 3, 4.



$\alpha = 0,9$

Vge IGBT top legs 1, 2, 3, 4



$\alpha = 0,5$

- Effective frequency at the output (and also in the DC-link HF filtering capacitors) = 4 times the IGBT switching frequency
- Enables to conciliate the need of high bandwidth and good filtering of the output current



I Out1 (Yellow) ; $\sum$ I Out (Red)
@ 350 A

❑ Determination of the transformer ratio

Linked to:

- Power availability needed during transients

Generation of the required current waveform with 20 kA/s di/dt → $U_{out\ max} / U_{out\ static} \sim 3$

- AC mains voltage variations < +/-10%
- Maximum duty cycle of PWM signals: 0,95
→ With PWM period = 60 μ s and IGBT leg dead time = 1 μ s, the minimum duration of the PWM pulses is 1 μ s (avoids pulse suppression by IGBT driver → Nonlinearities)
- Voltage drops accross the components

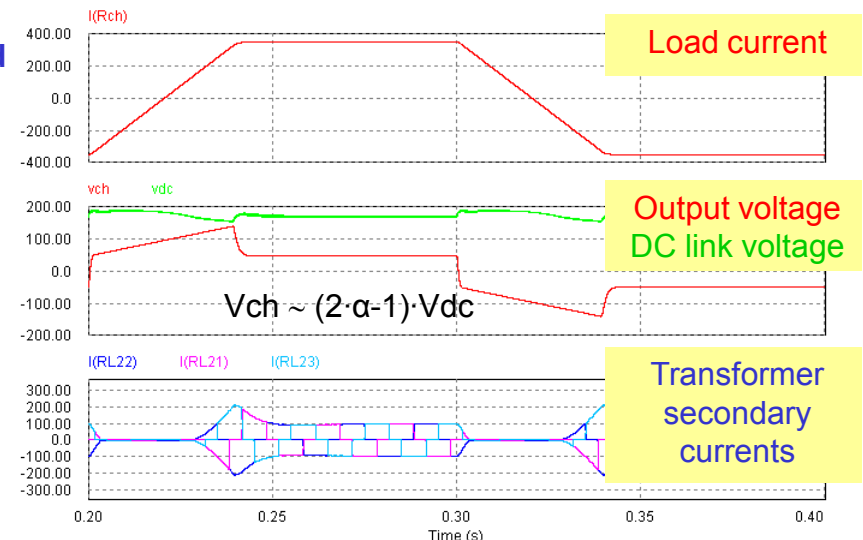
Ex: Transformer windings

→ $U_{secondary} @ I_{peak} \sim 92\%$. $U_{secondary} @ no\ load$

- Higher DC link voltage yields:
→ Increase of IGBT switching losses
→ Increase of output current distortion (IGBT dead time effect)



Transformer ratio = 6



Operation @ 5 Hz

Power converter sizing

❑ LC filter at the rectifier output:

- Resonant frequency: 25 Hz
- Attenuation of the 600 Hz harmonic: 30 dB

❑ IGBT switching frequency:

- Trade-off between efficiency, dynamic response and reliability

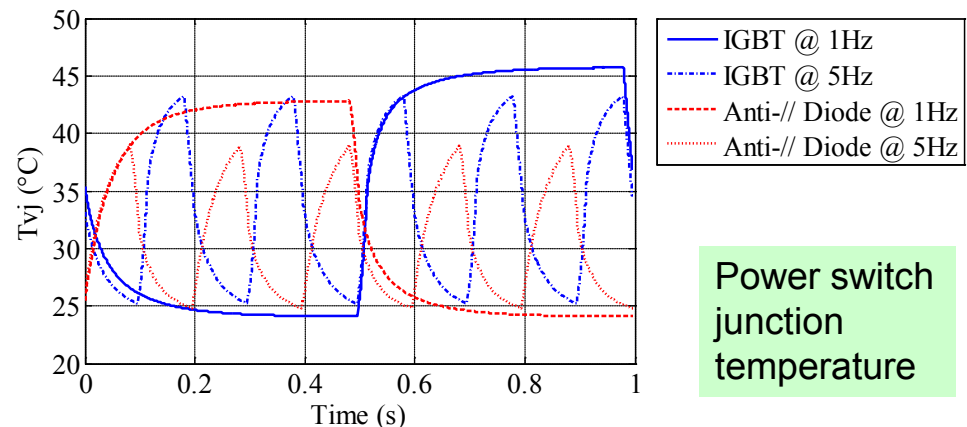
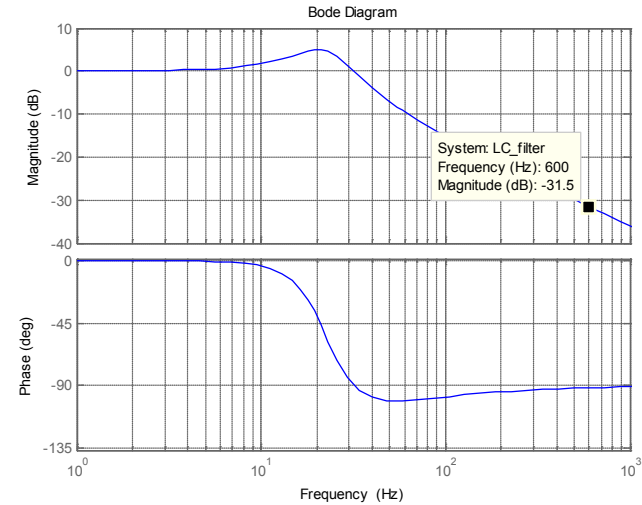
➡ 17 kHz

- IGBT modules: FF400R06KE3 from EUPEC
- Measured efficiency of the whole converter at nominal power: 85% (η inverter: 90%)

➤ Power cycling capability of the IGBT modules

Estimation using the power cycling curves provided by INFINEON for the 600V IGBT3 standard modules:

7.10¹⁰ cycles at 5 Hz operation
10⁹ cycles at less than 1 Hz operation



□ Output filter:

- - 3 dB cut-off frequency: 1500 Hz
- Peak gain: 2 dB
- Attenuation of 65 dB at 68 kHz (4 times the PWM frequency)

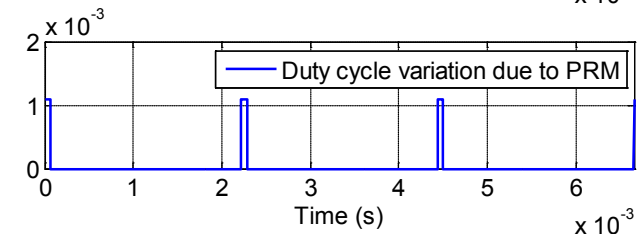
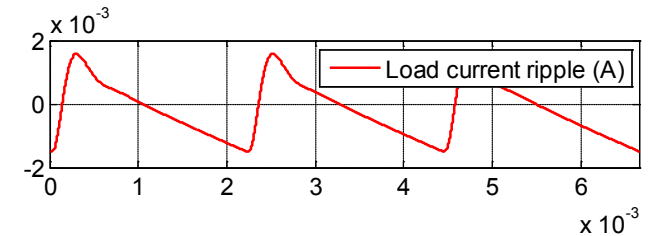
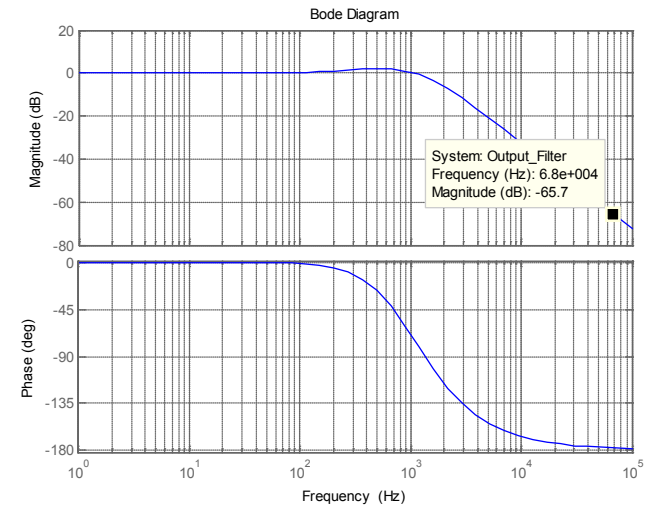
□ Influence on load current ripple of pulse repetition modulation (PRM) harmonics * :

- To overcome the resolution limits of classic digital PWM, a special pulse repetition modulation has been implemented by the Paul Scherrer Institute for the SLS controllers

➡ Generation of low frequency harmonics

- In our application, the PRM spectrum can contain subharmonics of the PWM carrier-frequency down to 450 Hz (1/37 of the PWM frequency)

**Output current distortion due to PRM harmonics
< 10 ppm of nominal**



Output current distortion due to
450 Hz harmonic

* F. Jenni, M. Emmenegger, "A Fully Digital PWM for Highest Precision Power Supplies", EPE 2001

❑ Current transducer:

➤ DCCT Ultrastab 866 – 600 DANFYSIK:

Linearity error < 1 ppm

Ratio error: Initial < 2 ppm / vs. Temperature < 0,3 ppm/°C

Offset error: Initial < 20 ppm / vs. Temperature < 0,2 ppm/°C

Output noise DC – 10 kHz < 0,05ppm

❑ Control electronics:



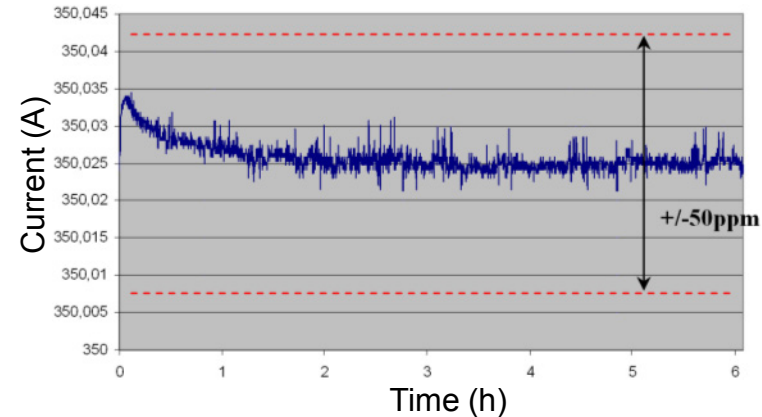
Use of SLS digital control cards *

➤ Already in use at SOLEIL on the 3 Hz Booster power supplies

➤ Well-proven and high performing electronics

➤ Training on the DSP and FPGA software dispensed by DIAMOND

➤ The whole converter can be controlled with a single control unit



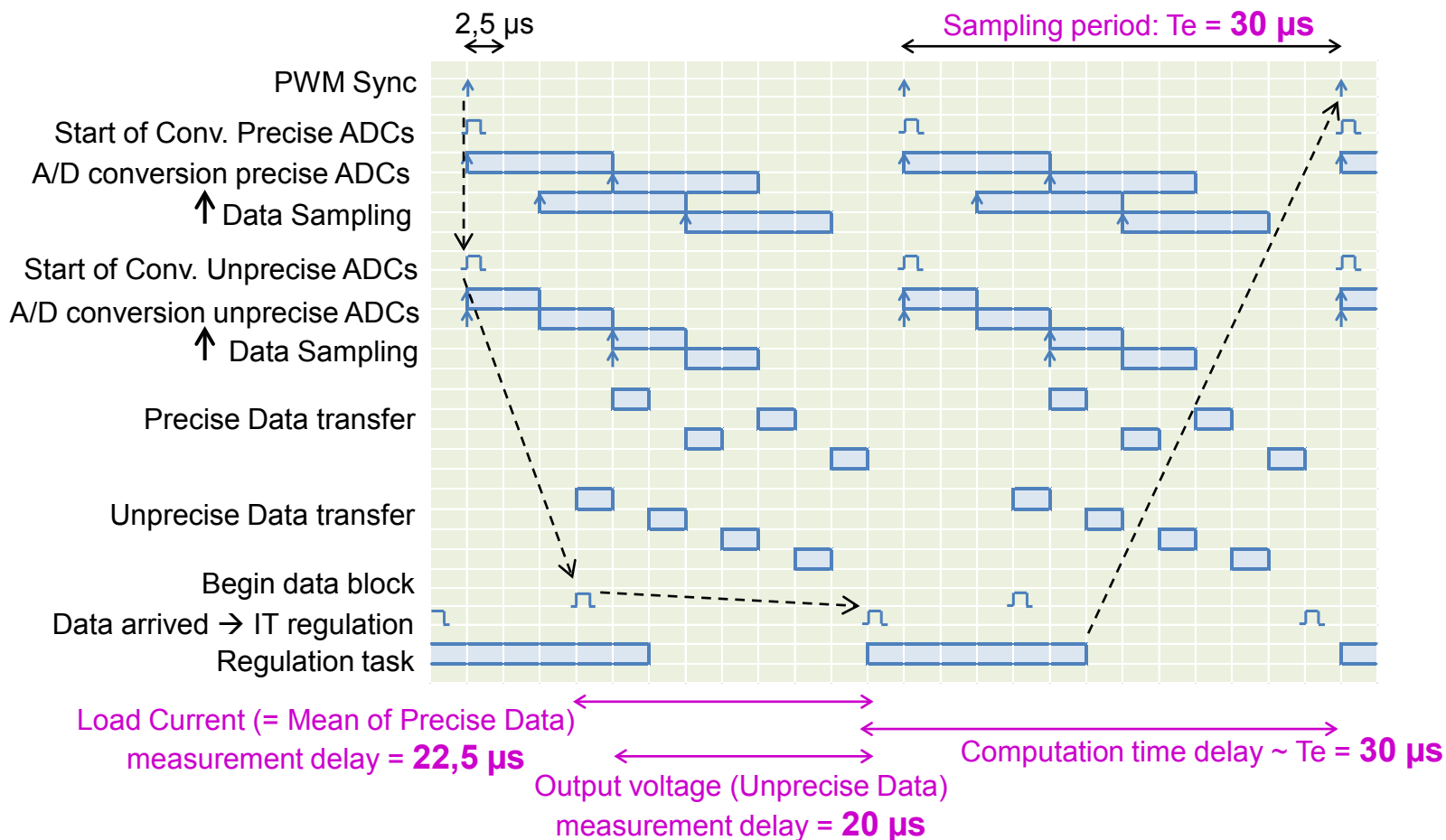
Current stability



* L. Tanner, F. Jenni, “Digital Control for Highest Precision Accelerator Power Supplies”, PAC’01

❑ Timing of PSI digital control cards:

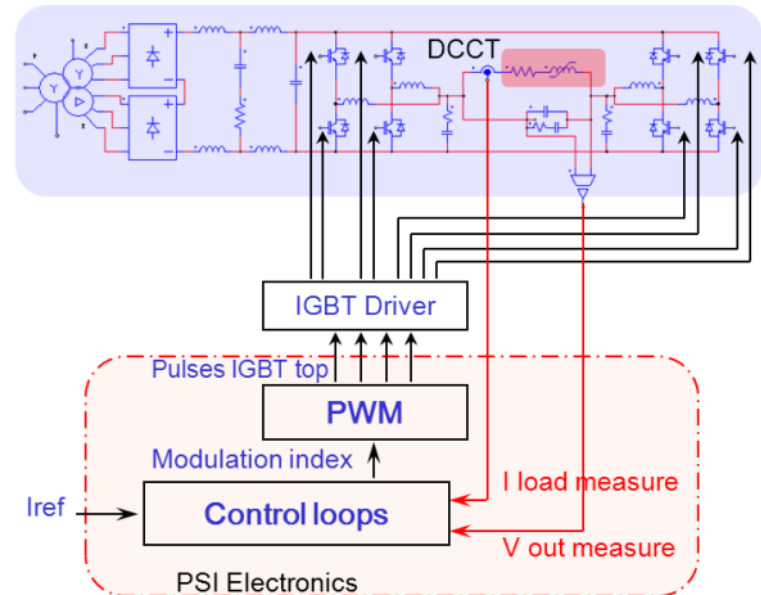
PWM Frequency = 17 kHz (60 μ s)



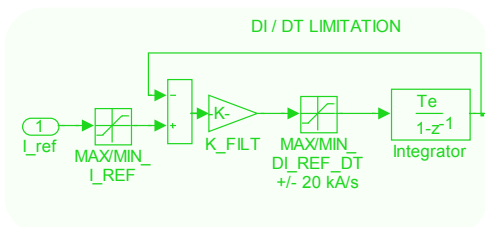
Control scheme

Based on 2 nested loops:

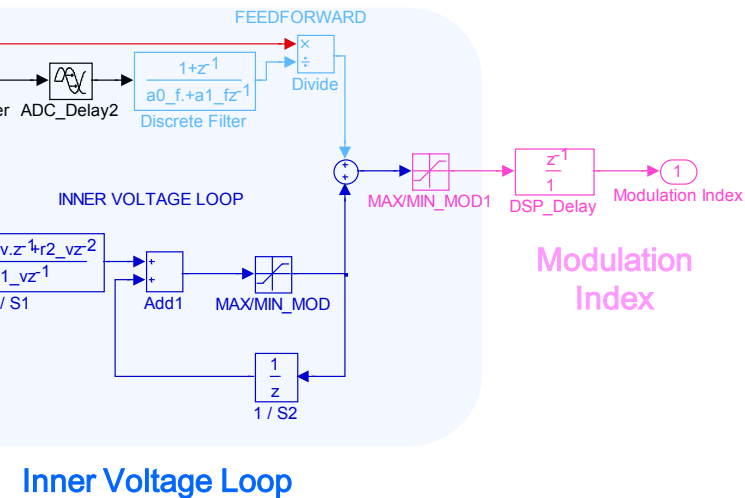
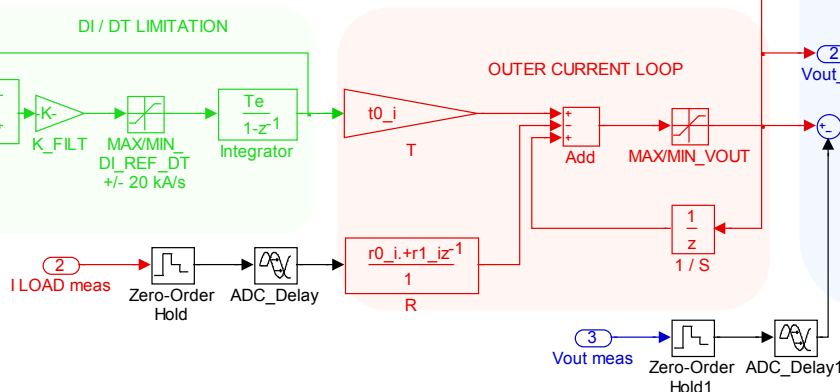
- **Fast inner voltage loop:**
PID controller + Feedforward
- **High precision outer current loop:**
PI controller implemented under a R.S.T form



di/dt Limitation +
rounded corners



Outer Current Loop



□ Voltage loop design * :

The power converter can be modelled by a second order system:

$$\frac{v_{out}}{m} = \frac{B_v(z^{-1})}{A_v(z^{-1})} = \frac{b0_v + b1_v \cdot z^{-1}}{1 + a1_v \cdot z^{-1} + a2_v \cdot z^{-2}}$$

Control delay:

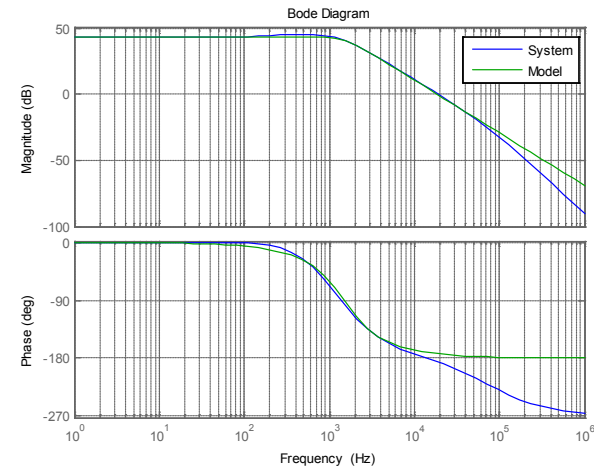
$$D(z^{-1}) = z^{-1} \cdot \underbrace{\left(\frac{z^{-1} + 2}{3} \right)}_{\text{Duty cycle computation delay}} \cdot \underbrace{\left(\frac{z^{-1} + 1}{2} \right)}_{\text{ADC delay} \cdot \text{Zero order hold delay}}$$

Closed-loop transfer function:

$$CL_v(z^{-1}) = \frac{D(z^{-1}) \cdot B_v(z^{-1}) \cdot R_v(z^{-1})}{A_v(z^{-1}) \cdot S_v(z^{-1}) + D(z^{-1}) \cdot B_v(z^{-1}) \cdot R_v(z^{-1})} \quad \text{where } \frac{R_v(z^{-1})}{S_v(z^{-1})} \text{ is the controller transfer function}$$



PID controller



* E. Godoy, E. Orstertag,
"A Complete Methodology for the Design of
a Digital Control Law for PWM Inverters",
EPE 2003

To limit the order of the controller, only the duty cycle computation time delay will be compensated.

The parameters of the controller are derived from a pole placement such that the voltage closed-loop behaves like a second order system with a cut-off frequency $F_{clv} = 2,5 \text{ kHz}$ (greater than the output filter resonant frequency) and a damping ratio $\xi_v = 0,7$:

$$A_v(z^{-1}) \cdot (1 - z^{-1}) \cdot S1_v(z^{-1}) + z^{-1} \cdot B_v(z^{-1}) \cdot R_v(z^{-1}) = 1 + d1_v \cdot z^{-1} + d2_v \cdot z^{-2}$$

An integrator is needed in the controller (zero steady-state error)

Computation time

$$d1_v = -2 \cdot e^{-\xi_v \cdot 2 \cdot \pi \cdot F_{clv} \cdot T_e} \cdot \cos\left(2 \cdot \pi \cdot F_{clv} \cdot T_e \cdot \sqrt{1 - \xi_v^2}\right)$$

$$d2_v = e^{-\xi_v \cdot 4 \cdot \pi \cdot F_{clv} \cdot T_e}$$

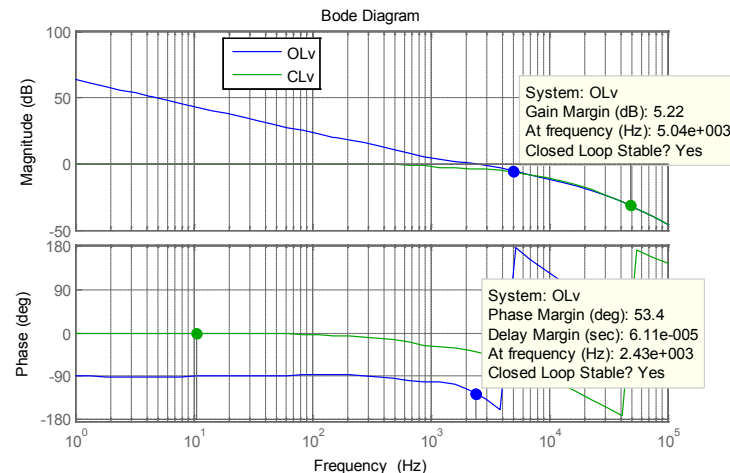
Order of the controller: 2

$$S_z(z^{-1}) = (1 - z^{-1}) \cdot S1_v(z^{-1}) = (1 - z^{-1}) \cdot (1 + s1_v \cdot z^{-1})$$

$$R_v(z^{-1}) = r0_v + r1_v \cdot z^{-1} + r2_v \cdot z^{-1}$$



Phase Margin: 50°
Gain Margin: 5 dB



Open and closed-loop Bode plots with power converter real transfer function

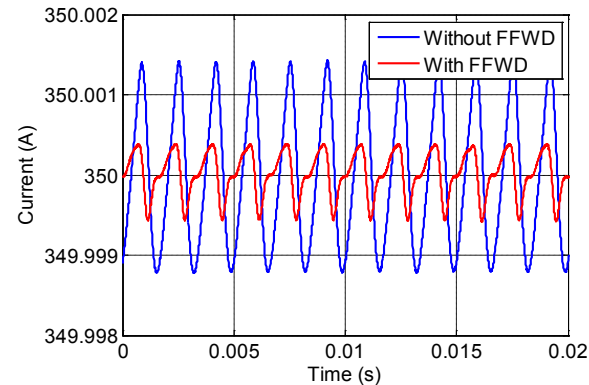
□ Feedforward control:

Improvement of dynamic and static behavior

$$Vdc_{FIL} = \frac{1 + z^{-1}}{a0_F + a1_F \cdot z^{-1}} \cdot Vdc_{MEAS} \rightarrow \text{High frequency filter (Cut-off frequency: 6 kHz)}$$

$$m(k) = \frac{Vout_{REF}(k)}{Vdc_{FIL}(k)}$$

⇒ 600 Hz ripple ÷ 4
< 5 ppm of nominal



□ Current loop design:

Computed considering that the voltage loop is unitary
(because of ratio between bandwidths of inner and outer loops)

System model with voltage loop:

$$\frac{I_{Load}}{Vout_{REF}} = \frac{B_i(z^{-1})}{A_i(z^{-1})} \approx Z \left(\frac{1}{Z_{Load}} \right) = \frac{b0_i + b1_i \cdot z^{-1}}{1 + a1_i \cdot z^{-1}}$$

Closed-loop: $CL_i(z^{-1}) \approx \frac{B_i(z^{-1}) \cdot T_i(z^{-1})}{A_i(z^{-1}) \cdot S_i(z^{-1}) + B_i(z^{-1}) \cdot R_i(z^{-1})}$

R_i, S_i, T_i polynomials → IP controller

Closed-loop pole placement method:

⇒ Solve $A_i(z^{-1}) \cdot S_i(z^{-1}) + B_i(z^{-1}) \cdot R_i(z^{-1}) = 1 + d1_i \cdot z^{-1} + d2_i \cdot z^{-2}$

Chosen cut-off frequency $F_{cli} = 700 \text{ Hz}$ → $F_{clv} / F_{cli} = 3,5$

Damping ratio $\xi_i = 1$

$$d1_i = -2 \cdot e^{-\xi_i \cdot 2 \cdot \pi \cdot F_{cli} \cdot T_e} \cdot \cos\left(2 \cdot \pi \cdot F_{cli} \cdot T_e \cdot \sqrt{1 - \xi_i^2}\right)$$

$$d2_i = e^{-\xi_i \cdot 4 \cdot \pi \cdot F_{cli} \cdot T_e}$$

@ $L = L_{\min} = 4 \text{ mH}$:
Phase Margin: 40°
Gain Margin: 13 dB

Order of the controller: 1

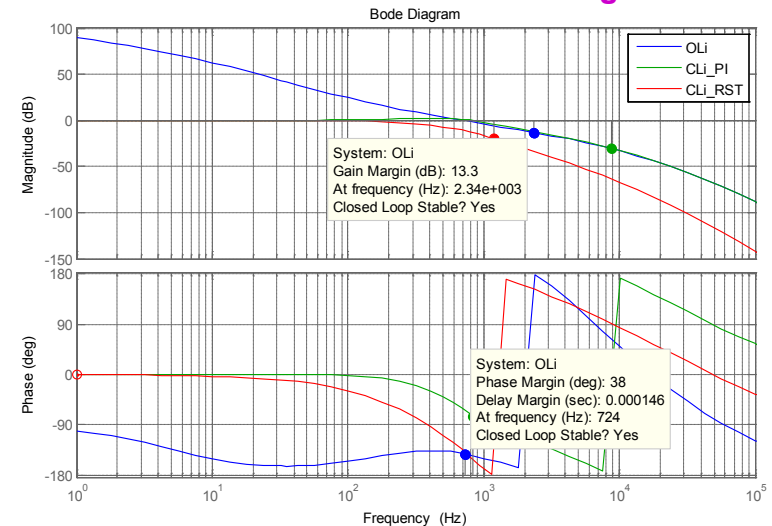
$$S_i(z^{-1}) = 1 - z^{-1}$$

$$R_i(z^{-1}) = r0_i + r1_i \cdot z^{-1}$$

Polynomial T_i :

- Chosen to assure unity gain to the closed-loop
- Designed so as to not introduce an undesirable zero in the closed-loop transfer function

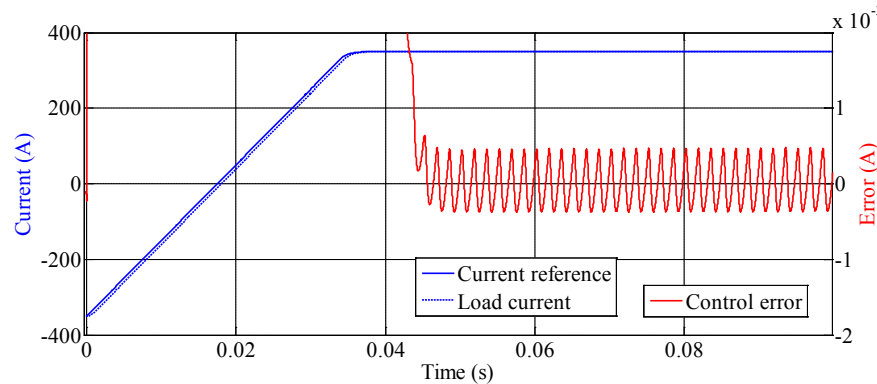
⇒ simple gain, directly given by the coefficients of $R_i(z^{-1})$: $T_i = r0_i + r1_i$



Open and closed-loop Bode plot with voltage closed-loop transfer function and control delays

➔ Tracking error in the ramps: @ $F_B = 0.35 / T_r$ (90% rise time), Phase shift $\sim 2,5^\circ$ (0,5 ms)

□ Simulation and experimental results:



Simulation of a current transition from -350 A to +350 A

- Current settling time ~ 50 ms
- Overshoot almost equal to zero
- Tracking error in the ramps ~ 3%

Ok in our application (1 ms synchronisation requirement between main and corrector power supplies), but could be improved by designing appropriate zeros in the closed-loop transfer function. Ex: Predictive algorithm estimating $I_{REF}(k+h)$ by using linear extrapolation:

$$T_i(z^{-1}) = (r0_i + r1_i) \cdot (1 + h - h \cdot z^{-1})$$

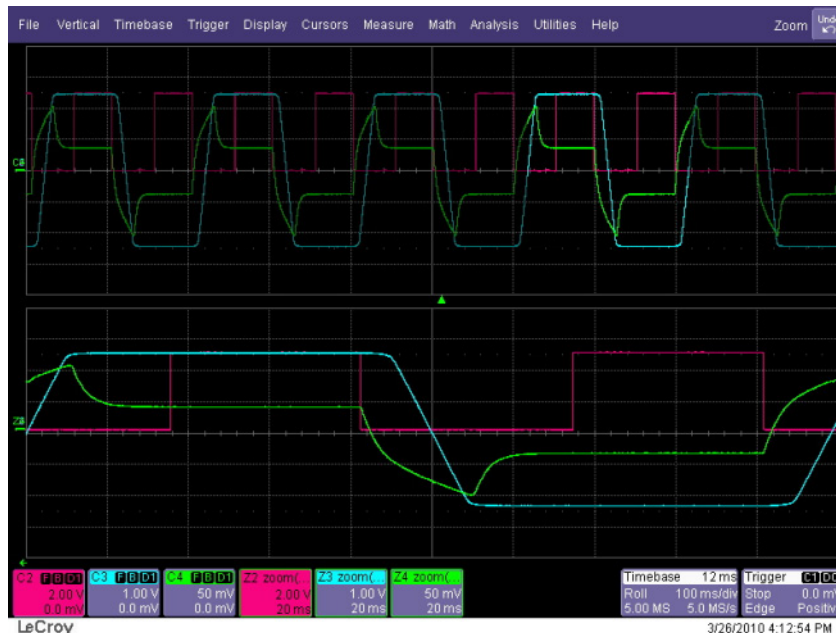
Operation @ 5 Hz on a 110 mΩ - 3 mH test load

Blue curve: Load current (150A/div)

Green curve: Output voltage (50V/div)

Red signal: High if control error below 100ppm of nominal

Time scale (Zoom window): 20ms/div



❑ Power tests with the undulator



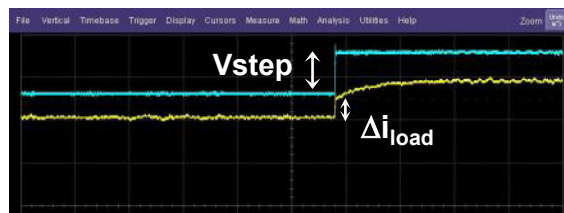
The control loop parameters had to be optimized to achieve stable operation

0 – 350 A variation

Yellow curve: Load current

Blue curve: Output voltage

Green signal: High if control error below 100ppm of nominal



Voltage step

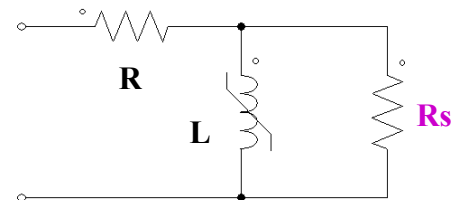
Yellow curve: Load current

Blue curve: Output voltage



$$R_s = V_{step} / \Delta i_{load} - R = 140 \text{ m}\Omega$$

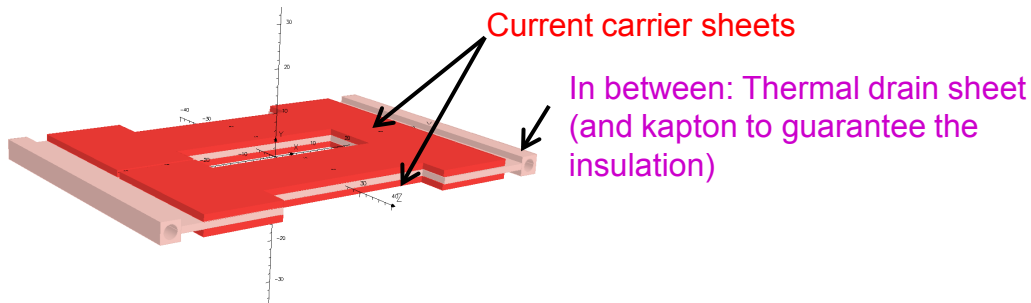
Equivalent circuit of the real load:



□ Explanation:

Results from the structure of the coils.

Each of them = 25 layers of copper stacked together around the poles, among 9 are cooling plates

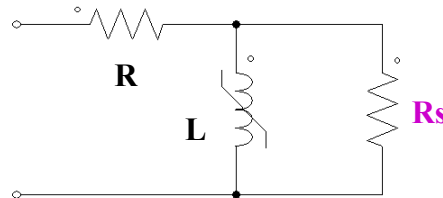


View of elementary coil



Equivalent model of the undulator = Transformer which secondaries are short-circuited.

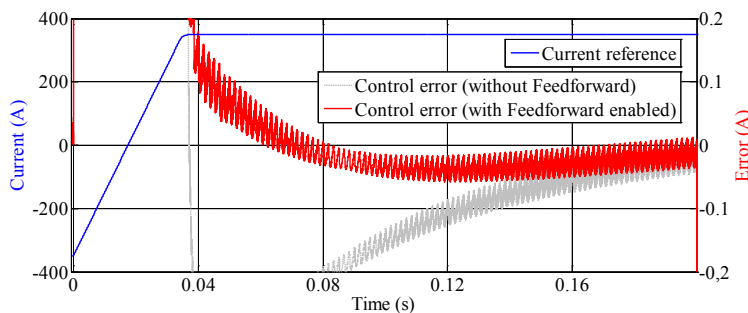
Seen from the primary, the model classically becomes:



$$R_s = 9 \cdot \frac{\rho \cdot l}{S} \cdot \left(\frac{16}{9} \right)^2 = 140 m\Omega$$

R_s : secondary winding resistance reflected to the primary side

The power supply dynamic performances can be improved by adding a feedforward term to the current controller output :

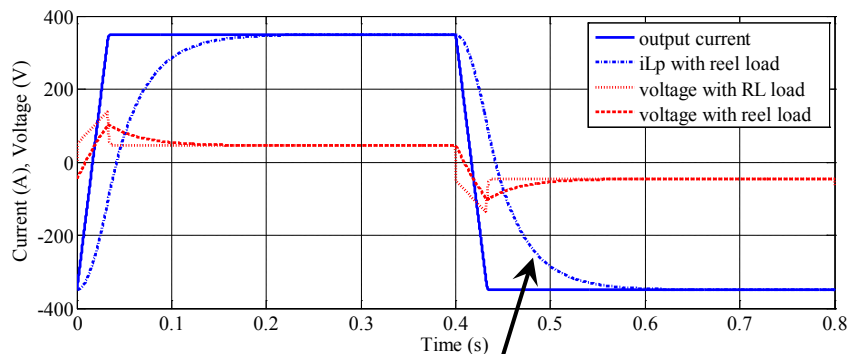


$$v_{REF}(k) = Z_{EST}(i_{REF}(k)) \cdot i_{REF}(k)$$

$$Z_{EST} = \frac{R + R_s + R \cdot R_s \cdot T_e / L(i_{REF}) - (R + R_s) \cdot z^{-1}}{1 + R_s \cdot T_e / L(i_{REF}) - z^{-1}}$$

where Z_{EST} is the estimation of the load impedance

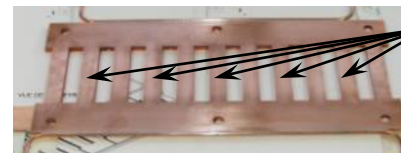
However, a serious issue lies in the magnetic field settling time → About 300 ms



Current flowing through the load primary inductance ~ image of the magnetic field

Output waveforms in AC mode of operation

To overcome this problem, the thermal drain sheets (TDS) are currently under modification to increase the resistance value of the load secondary circuit:

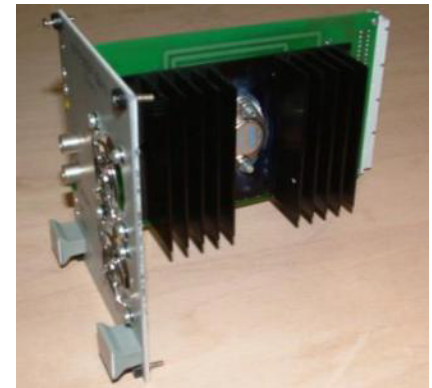
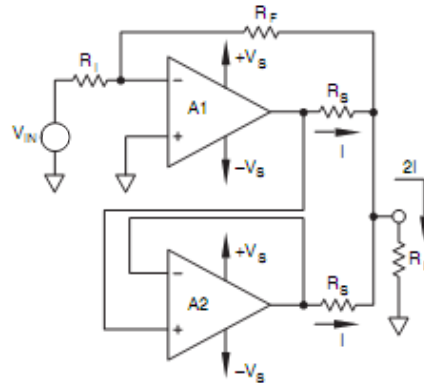
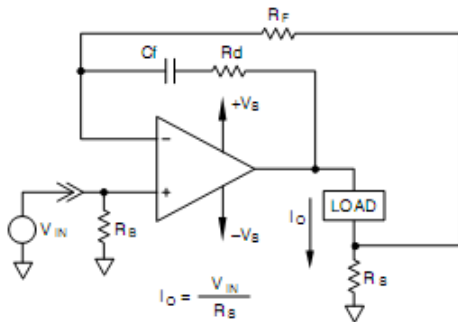
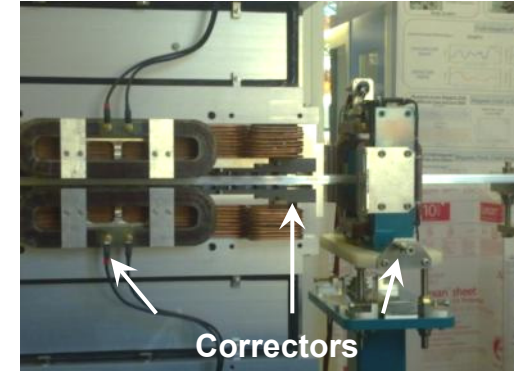


Insertion of gaps in the TDS

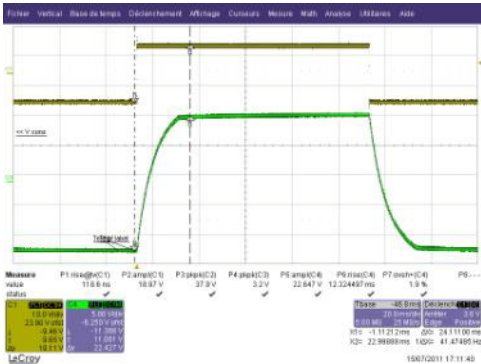
With the gaps, the total magnetic field which crosses each TDS window (then surrounding 2 adjacent poles instead of only 1) is zero. With a resistance increase by a factor of at least 10, the 100 ms target for the magnetic field settling time can be reached.

Corrector power supply design

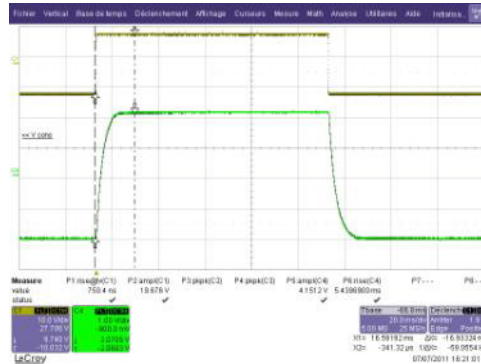
- ❑ A set of 8 bipolar power supplies is needed to feed the correction coils split between the entrance and the exit of the undulator.
- ❑ These correctors are necessary to keep the field integral as low as possible during the main field transitions and to maintain the beam trajectory on the reference orbit.
- ❑ Power supplies rated between 10 A / 100W and 20 A / 200 W
- ❑ **Structure:**
Based on the use of either single ou paralleled power operational amplifiers (PA12A from APEX)



- Current settling time: ~ 15 ms (load time constant ~ 3 ms)



± 10 A / ± 10 V power supply

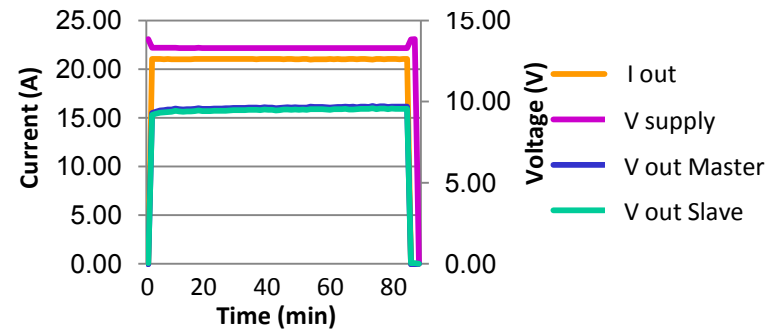


± 20 A / ± 10 V power supply

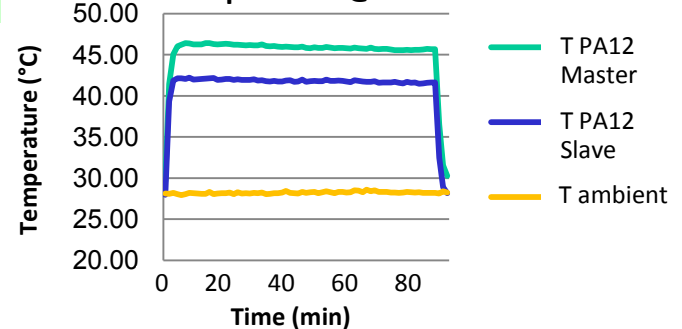
- In order to drive the corrector PS synchronously with the main PS, a special device has been developed. It consists of:
 - a 80 MHz μ C on which the correction tables are shipped
 - fast ADCs which generate @ a 1 kHz rate the analog setpoint signals driving each of the 9 power supplies

➔ The 1 ms synchronisation requirement between the power supplies is met

Waveforms @ 21 A

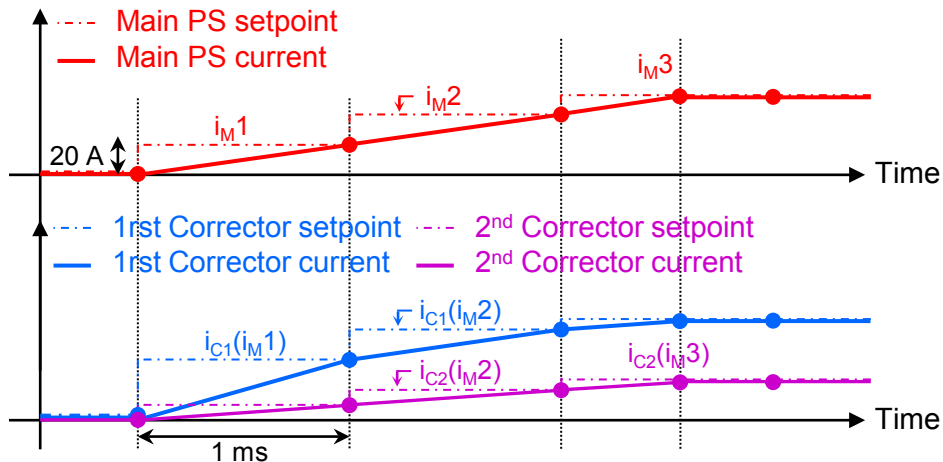


Temperature @ 21 A



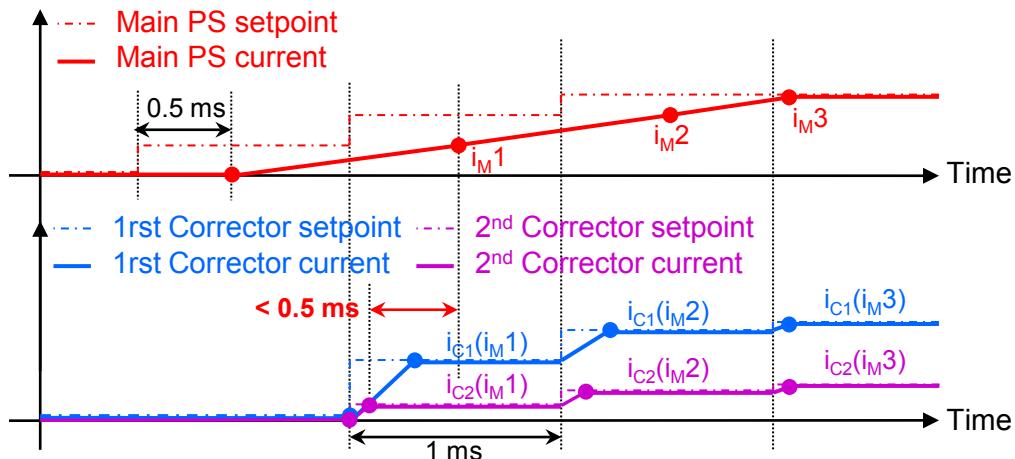
ID Feedforward compensation

□ Ideal waveforms during changes of the main magnetic field:



- Step by step feedforward tables: To each main PS current value corresponds a set of corrector current values
- Ideal compensation: The 9 power supplies begin ramping to the new setpoints synchronously and reach these setpoints at the same instants

□ Real waveforms:



- The current slope of the power supplies is constant (unlike the corrector current steps) → the 9 power supplies do not reach their present setpoints at the same time
- Suppression of (most of) the transitory effects on the beam position caused by this imperfect FFWD compensation

➤ SOLEIL Fast Orbit Feedback correction system *

* L-S. Nadolski et al., "Beam Position Orbit Stability Improvement at SOLEIL", PAC'09

Questions



**Thank you for your attention.
Questions ?**

