SOFTWARE UPGRADE OF DSP AND FPGA CONTROL SYSTEMS FOR J-PARC LINAC

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Abstract

For the proton linear accelerator (LINAC) at the Japan Proton Accelerator Research Complex (J-PARC), the RF fields at acceleration RF cavities are controlled by an FPGA (Field-Programmable Gate Array)-based digital feedback (FB) control system installed in a compact PCI (cPCI). Recently, the software of DSP and FPGA programs for the low-level RF (LLRF) control systems of the J-PARC LINAC is upgraded. Firstly, a function of inspecting cavity pickup and cavity reflection signals is added to the LLRF control systems so that any of instabilities could be monitored in real-time, and an interlock due to larger RF cavity reflection amplitude will be applied to the fast interlock sysem. Secondly, an intelligent sag compensation and automatic FPGA calibration are programmed so that the RF wavforms in case of FB OFF and FB ON can be almost the same. Furthermore, a new function of separating the chopped beam automatically to two scrapers is being developed using FPAG control systems. The details on the software upgrade of the DSP and FPGA programs will be reported in this paper.

INTRODUCTION

The J-PARC LINAC is operated at a repetition rate of 25 Hz with a beam pulse width of 500 μs. After installing the 972-MHz high-β accelerator section into the J-PARC LINAC behind the 324-MHz low-β section, the proton beam energy was successfully upgraded to 400 MeV in January 2014. For the 400-MeV LINAC, there are 48 RF stations and 64 cavities in total. For each RF station, one RF source is used to feed RF power to the RF cavities. In the 324-MHz low-β section, three solid status amplifiers and twenty 324-MHz klystrons are used as the RF sources. In the 972-MHz high-β section, twenty five 972-MHz klystrons are used. For each RF source, a low level RF (LLRF) control system unit is applied [1-2].The RF signals including the RF amplitude and phase at the RF cavities are controlled by an FPGA (Field-Programmable Gate Array)-based digital feedback (FB) control system installed in a compact PCI (cPCI) [3-4]. Recently, the software of DSP and FPGA programs for the low-level RF (LLRF) control systems of the J-PARC LINAC is upgraded.

FUNCTION OF INSPECTING CAVITY PICKUP AND CAVITY REFLECTION SIGNALS

The digital feedback (FB) control system installed in a compact PCI (cPCI) is applied to the low level RF (LLRF) control systems of the J-PARC LINAC. In the 972-MHz high-β accelerator section, each klystron feeds RF power to one ACS (Annular Coupled Structure) cavity. The block diagram of the RF feedback control for 972-MHz RF station is shown in Fig. 1. The compact PCI (cPCI) consists of a CPU (Central Processing Unit), an IO (Input/Output), a DSP (Digital Signal Processor) with FPGA, a Mixer&IQ (Mixer & IQ-modulator), and an RF&CLK (Clock) board [3-4].

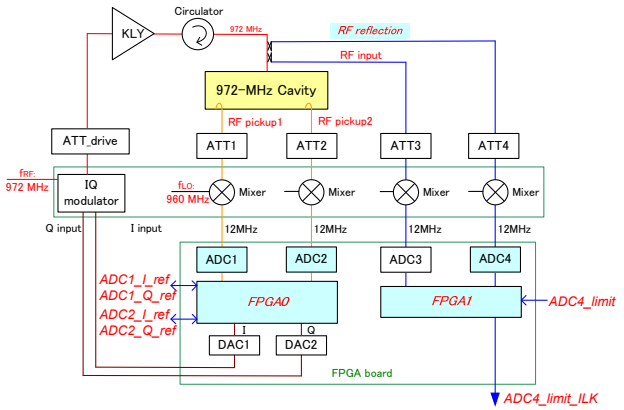

Figure 1: Block diagram of the RF feedback control for 972-MHz RF station.

In the RF&CLK board, RF (972 MHz), LO (Local Oscillator, 960 MHz), and clock (48 MHz) signals are generated. The LO (960 MHz) output signals from the RF&CLK board will be used in the down-converters (Mixers) to detect the RF signals from the RF cavity. The output signals with an intermediate frequency (IF) of 12 MHz from the down-converters will be acquired directly by the ADCs in the FPGA board. The sampling frequency of the ADCs is 48 MHz. Two pickup signals, one RF input signal, and one RF reflection signals of the ACS cavity, will be detected by the 4 ADCs in the FPGA board as shown in Fig. 1. One FPGA board consists of two FPGAs (Xilinx XC2V2000). The FPGA0 is used for real-time feedback processing of the accelerating field. After separating the I (in-phase) and Q (quadrature) components from the IF signals for the two cavity pickup signals, a PI (Proportional-Integral) feedback control is conducted to obtain a stable RF field at the RF cavity. The FPGA1 is used for measuring I and Q components of the RF input and reflection signals of the RF cavity. All of the RF signal data will also be sent to the DSP (Digital Signal Processor).

Besides measuring the I and Q components of the RF

signals, recently a function of inspecting RF cavity reflection amplitude and RF cavity pickup signals in real-time are added into the LLRF control systems.

At first, the function of inspecting RF cavity reflection amplitude (*ADC4_amp*) is conducted by comparing with a limit setting (*ADC4_limit*) which is set beforehand. In the case of the reflection amplitude (*ADC4_amp*) larger than the limit setting (*ADC4_limit*), namely, *ADC4_amp* > *ADC4_limit,* the DAC output will be reset to 0 so as to protect the RF systems. In the meantime, an interlock signal (*ADC4_limit_ILK*) will come out: *ADC4_limit_ILK* = 1. Furthermore, this interlock signal *(ADC4_limit_ILK*) will be applied to the fast interlock sysem to stop beam for protecting the accelerator.

On the other hand, the function of inspecting RF cavity pickup signals (*ADC1_I/Q* and *ADC2_I/Q*) during feedback ON is carried out by comparing with a reference setting (*ADC1_I/Q_ref* and *ADC2_I/Q_ref*) which is saved beforehand during normal operation with FB ON. Then, if cavity pickup signal is far away from the reference setting, for example, *ADC1_I- ADC1_I_ref* > 50*,* all of the ADC data for cavity pickups, input, and reflection, and DAC data, will be saved for later investigations on the RF systems. By using this function, any of instabilities of the RF cavity pickup signals during FB ON could be monitored in real-time for our RF systems.

INTELLIGENT SAG COMPENSATION AND AUTOMATIC FPGA CALIBRATION

For the J-PARC LINAC the beam is operated in a pulse mode with a width of 500 μs. The pulsed high voltage applied to klystron is of a width of 700 μs for 324-MHz RF stations, and 650 μs for 972-MHz RF stations, respectively. There is a sag in the flat top of the high voltage waveform. Thus, the RF output waveform from klystron to cavity also drops in the flat top with FB OFF, as shown in the blue curve in Fig. 2. Recently, an intelligent sag compensation is being carried out by using the DSP control program.

At first, a sag coefficient for amplitude and phase ($\Delta\alpha\_test$ and $\Delta\phi\_test$) is measured by detecting the amplitude (A_{t1} and A_{t2}) and phase (ϕ_{t1} and ϕ_{t2}) of RF cavity pickup signals at two sampling points (*T_sag_start* and *T_sag_stop*),

$$\Delta\alpha\_test = \frac{\frac{A_{t2}-A_{t1}}{t_2-t_1}}{\frac{A_{t1}+A_{t2}}{2}};$$

$$\Delta\phi\_test = \frac{\phi_{t2}-\phi_{t1}}{t_2-t_1},$$

where t_1 = *T_sag_start*, and t_2 = *T_sag_stop*.

Then, a correct sag compensation coefficient for amplitude and phase ($\Delta\alpha$ and $\Delta\phi$) is calculated out as,

$$\Delta\alpha = \Delta\alpha_0 + \Delta\alpha\_test;$$
$$\Delta\phi = \Delta\phi_0 + \Delta\phi\_test,$$

where $\Delta\alpha_0$ and $\Delta\phi_0$ are sag compensation coefficients which was already set in the LLRF control systems.

Finally, the correct sag compensation coefficient will be applied to DSP program for generating a feed-forward setting table of I and Q components (*FF_I_t* and *FF_Q_t*) as the following,

$$FF\_I\_t = A\_t \times \left[1-\Delta\alpha(t-\frac{t_1+t_2}{2})\right]\cdot\cos\left[\theta-\Delta\phi(t-\frac{t_1+t_2}{2})\right];$$

$$FF\_Q\_t = A\_t \times \left[1-\Delta\alpha(t-\frac{t_1+t_2}{2})\right]\cdot\sin\left[\theta-\Delta\phi(t-\frac{t_1+t_2}{2})\right],$$

where t is from 0 to 1023 μs, and A_t and θ are the amplitude and phase of reference setting, respectively. After sag compensation, the amplitude and phase at the flat top of RF output signals from klystron to cavity will be a constant even with FB OFF, as shown in the red curve of Fig. 2.

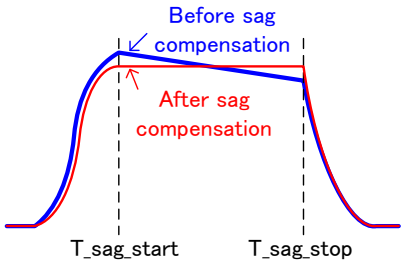

Figure 2: RF amplitude waveform with FB OFF before and after sag compensation.

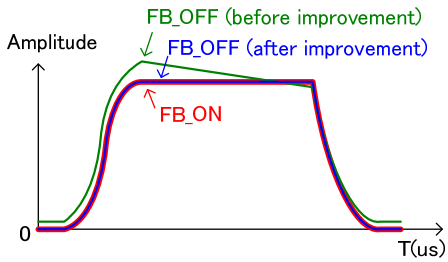

Figure 3: RF amplitude waveform with FB OFF and FB ON.

Moreover, by applying an automatic FPGA calibration as following, the same RF field will be obtained for FB OFF and FB ON, as shown in Fig. 3.

DAC_amp_cali_new=Amp_ref/ADC_amp×DAC_amp_cali_old;
DAC_pha_cali_new=Pha_ref-ADC_pha+DAC_pha_cali_old,

where, *DAC_amp_cali_new* and *DAC_pha_cali_new* are the correct calibration parameters for DAC amplitude and phase, *DAC_amp_cali_old* and *DAC_pha_cali_old* are the old calibration parameters for DAC amplitude and phase, *Amp_ref* and *Pha_ref* are the amplitude and phase of FB reference setting, and *ADC_amp* and *ADC_pha* are the amplitude and phase of ADC.

By using the functions of intelligent sag compensation and automatic FPGA calibration, the RF power in the cavity will not change with FB switching between ON and OFF, and they are very helpful for accelerator operation, especially for switching operation mode between RF cavity conditioning and beam acceleration.

FUNCTION OF SEPARATING CHOPPED BEAM AUTOMATICALLY TO TWO SCRAPERS

At the J-PARC LINAC, presently one scraper is used as dump of chopped beam after the chopper. However, we are planning to increase the proton beam current from 20 to 50 mA in the soon future, and the beam power will be over the limitation of the scraper. Therefore, two scrapers will be applied after the chopper.

Then, a function of separating the chopped beam automatically to the two scrapers is considered by using FPGA program in the LLRF control systems. Figure 4 shows the schematic diagram of one chopper with two scrapers at the J-PARC LINAC. Moreover, two ways for separating beam are considered: 1) separating beam by macro-pulse of RF gate signals, and 2) separating beam by intermediate-pulse of chopping signals.

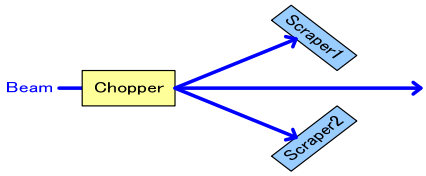

Figure 4: Schematic diagram of one chopper with two scrapers at the J-PARC LINAC.

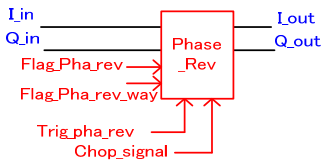

Figure 5: Phase-reversion function block inserted in the FPGA output circuits.

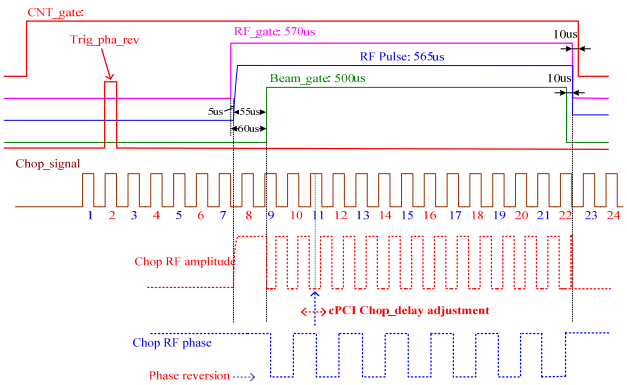

Figure 6: Schematic view of timing signals for chopper station, and RF amplitude and phase of the chopper output.

In order to realize the function of separating beam, a phase-reversion function block is inserted in the FPGA output circuits for the FPGA program as shown in Fig. 5. In Fig. 5, there are two timing input signals to the phase-reversion function block. One input signal is "Trig_pha_rev", which is a trig signal with a repetition rate of 12.5 Hz used for the first way: separating beam by macro-pulse of RF gate signals. The other input signal is "Chop_signal", which is used for the second way: separating beam by intermediate-pulse of chopping signal. Then, in Fig. 5, the separating way is decided by the input parameter "Trig_pha_rev_way" which is defined on the touch panel (TP) of the PLC (Programmable Logic Controller) of the LLRF control system. Furthermore, a switch "Trig_pha_rev" is also set by the PLC TP for turning this function ON or OFF.

Figure 6 shows a schematic view of timing signals for chopper station, and RF amplitude and phase of the chopper output for separating beam by intermediate-pulse of chopping signal. The chopped beam separation is realized by using the FPGA program. All of the input timing signals and reversion setting shown in Fig. 5 and Fig. 6 will be detect by the FPGA, and a phase reversion of the I and Q output signals is carried out tracking all of the input signals including the chopping signal in real time. The RF phase reversion can be easily taken out by using $I\_out=-I\_in$, and $Q\_out=-Q\_in$. Thus, the beam will be chopped to a revered direction so that the beam is separated to two scrapers. Of course, we need to adjust the chopping-signal delay once before the application of the system to the beam operation in order to assure that the timing of the phase reversion is at the bottom of the RF amplitude. By using this design, we can see that, the above two ways for beam separation becomes available in one control system and could be chosen easily just with one button on the PLC TP.

SUMMARY

Software for the DSP and FPGA programs is upgraded. By applying function of inspecting cavity pickup and cavity reflection signals, instabilities could be monitored in real-time, and an interlock due to larger RF cavity reflection amplitude could be applied to the fast interlock sysem. With intelligent sag compensation and automatic FPGA calibration, the RF wavforms in case of FB OFF and FB ON could be almost the same. Furthermore, a new function of separating the chopped beam automatically to two scrapers is being developed using FPAG control systems.

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