CSNS Timing System

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Contents of this talk

- Brief introduction to CSNS
- Requirement investigation
- Strategy: based on event timing concept
- Progress
- Challenges
Layout design based on the geology detection last year
Accelerator beam power front

Jie Wei

![Graph showing the relationship between kinetic energy and average beam current for various beam facilities. The graph includes points for existing and under construction facilities, with different symbols indicating different types of configurations.](image-url)
**Beam Travel Length**
- FE: 9m
- DTL: 38.13m
- LRBT: 170.5m
- RSC: 238.8m
- RTBT: 123m

**RCS**
- 1.6 GeV, 25Hz
- $63/125 \, \mu A$

**CSNS Timing System**

\[ P_B = 100/200kW \]
CSNS baseline layout

- H- IS, 50 keV, $I_p = 20$ mA
- Room for higher energy linac
- RFQ, 3 MeV, 324 MHz
- DTL, 80 MeV, $I_{ave} = 75$ µA
- Future medical applications
  - RCS 1.6 GeV, 25 Hz, 63 µA
  - Future proton applications
  - To future second target, muon target, fast neutron

Target station & neutron instruments
Requirement investigation

- H-
- RFQ
- DTL-RF
- Inj. Bumpers
- RCS RF
- RCS PS
- Ext. Kickers
- Choppers

8 sets

8 sets

10 sets
CSNS timing task (1)

- Scheduled timing
  - H-source
  - magnet power supply,
  - injection bumpers and extraction kickers
  - beam diagnostics
  - Linac and RCS RF
  - Target and detectors
CSNS timing task (2)

• Synchronized timing
  – Triggers to LEBT /MEBT chopping should be synchronized with RCS RF phase
  – Triggers to extraction kickers should be synchronized with RCS beam
CSNS timing task (3)

- **Synchronizing clock**
  - 1MHz clock for magnet power supply

- **RF reference distribution**
  - to linac LLRF and BI

- **Timestamp and some operating related parameters distributed through dedicated event timing links**
## Requirement for triggers

<table>
<thead>
<tr>
<th>sys</th>
<th>device</th>
<th>num</th>
<th>delay Ch</th>
<th>pulse width</th>
<th>Max. Freq</th>
<th>rising time</th>
<th>jitter (RMS)</th>
<th>delay scope</th>
<th>adjust step</th>
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<tr>
<td>PS</td>
<td>DTL-Q</td>
<td>76</td>
<td>76</td>
<td>10us</td>
<td>25Hz</td>
<td>&lt;10ns</td>
<td>&lt;100ns</td>
<td>&lt;40us</td>
<td>100ns</td>
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<td></td>
<td>RCS-B</td>
<td>1</td>
<td>1</td>
<td>10us</td>
<td>25Hz</td>
<td>&lt;10ns</td>
<td>&lt;100ns</td>
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<td>100ns</td>
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<td></td>
<td>RCS-Q</td>
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<td>&lt;100ns</td>
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<td>100ns</td>
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<td>100ns</td>
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<td>RCS RF</td>
<td>LLRF</td>
<td>14</td>
<td>14</td>
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<td>25Hz</td>
<td>&lt;10ns</td>
<td>&lt;100ns</td>
<td>&lt;40us</td>
<td>100ns</td>
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<td>Inj. Ext.</td>
<td>bumper</td>
<td>2</td>
<td>2</td>
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<td>50Hz</td>
<td>5ns</td>
<td>1ns</td>
<td>1ms</td>
<td>5ns</td>
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<td>kicker</td>
<td>10</td>
<td>10</td>
<td>1us</td>
<td>50Hz</td>
<td>5ns</td>
<td>1ns</td>
<td>1ms</td>
<td>5ns</td>
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<td>25Hz</td>
<td>1us</td>
<td>1us</td>
<td>&lt;40us</td>
<td>100ns</td>
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<td>linac LLRF</td>
<td>sys start</td>
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<td>9</td>
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<td>&lt;100ns</td>
<td>&lt;40us</td>
<td>100ns</td>
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<td>RF GATE</td>
<td>9</td>
<td>9</td>
<td>200us ~ 800us</td>
<td>25Hz</td>
<td>&lt;10ns</td>
<td>&lt;100ns</td>
<td>&lt;40us</td>
<td>100ns</td>
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<td></td>
<td>mod gate</td>
<td>9</td>
<td>9</td>
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<td>25Hz</td>
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<td>&lt;100ns</td>
<td>&lt;40us</td>
<td>100ns</td>
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<td>H-source</td>
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<td>300us</td>
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<td>&lt;100ns</td>
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<td>100ns</td>
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<td>&lt;10ns</td>
<td>&lt;100ns</td>
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<td>&lt;100ns</td>
<td>&lt;40us</td>
<td>100ns</td>
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<td>&lt;100ns</td>
<td>&lt;40us</td>
<td>100ns</td>
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</table>
Strategy: adopting event timing concept

- RF input
  - 50/60 Hz TTL input
- Hardware triggers / Clocks
- Event Generator

Fan-Out FOUT-7/FOUT-24

Event Receiver

Event Receiver

Four-Channel Timer

Event Receiver

E-Gun Transmitter

E-Gun Receiver
Event timing system

- Functionality based on the APS timing system
- Redesigned for SLS → Series 100
- Improved performance for Diamond → Series 200
- Timing signals needed for synchronisation of subsystems are applied to Event Generator (EVG) or generated by EVG
- Timing information is converted to 8-bit event codes and distributed to Event Receivers (EVR) as optical signals
- Event clock rate determines timing resolution:
  - Minimum clock rate 50 MHz, 20 ns resolution
  - Maximum clock rate 125 MHz, 8 ns resolution
- 8-bit distributed bus running in parallel and independent of timing events allows distribution of eight signals updated with the event clock rate
Strategy: adopting event timing concept

- Event Generator (EVG), Event Receiver (EVR)
- Multi-mode optical fiber between EVG and Fanout/EVR
- 8 bit event codes and 8 clock
- Timestamp and data buffer
- Heartbeat monitor
- Interlock input to disable some outputs
- Fine grained adjustable output pulses and clock frequencies.
Design the CSNS timing system using EVG/EVR

Using experience of BEPCII timing system, but requirements different

- Decide the event clock
  - \( \frac{324\text{MHz}}{4} = 81\text{MHz} \)

- Calculate the parameters for Fractional-N synthesizer
  - Work out several equations and inequalities
Fractions Synthesiser

- A Micrel (http://www.micrel.com) SY87739L Protocol Transparent Fractional-N Synthesiser with a reference clock of 24 MHz is used in EVG. By correctly setting the parameters in this circuit, we can get proper frequency for CSNS timing system.
Calculate parameters of Fractional-N synthesizer

\[ f_{\text{VCO}} \text{ (min)} = 540\text{MHz}, \ f_{\text{VCO}} \text{ (max)} = 729\text{MHz} \]

\[ f_{\text{FOUT}} = \left[ P - \frac{Q_{P-1}}{Q_P + Q_{P-1}} \right] \times f_{\text{REF}} \]

\[ f_{\text{VCO}} \text{ (min)} < f_{\text{REF}} \times \left\{ P - \left[ \frac{Q_{P-1}}{(Q_{P-1} + Q_P)} \right] \right\} < f_{\text{VCO}} \text{ (max)} \]

\[ 540\text{MHz} \leq f_{\text{WOUT}} = \frac{N}{M} \times f_{\text{FOUT}} = \frac{N}{M} \times \left[ P - \frac{Q_{P-1}}{Q_{P-1} + Q_P} \right] \times f_{\text{REF}} \leq 729\text{MHz} \]
Calculate parameters of Fractional-N synthesizer

- \( f_{\text{ref}} = 24 \text{MHz}, \) event clock = 81MHz
- \( 24 \times (P - Q_{p-1}/(Q_{p-1} + Q_p)) / \text{PostDivSel} = 81, \)
  \( 540 < 24 \times (P - Q_{p-1}/(Q_{p-1} + Q_p)) < 729, \)
- \( P = 24, \) \( Q_{p-1} = 3, \) \( Q_p = 5, \) \( \text{PostDivSel} = 7, \) \( N = M = 14 \)
- \( 0000 \ qp \ qpm1 \ divsel \ 000 \ PostDivSel \ NdivSel \ MdivSel \)
  \( 0000 \ 00101 \ 00011 \ 0111 \ 000 \ 00111 \ 101 \ 101 \)
  \( = 0x028d \ c1ed \)
Progress (cont.)

- Very preliminary design
- Prototype 1
  - Got official approval
  - Hardware ordered but not reached us
  - Several experiments done using BEPCII spare parts
324MHz measured from EVR230, done by Guanglei Xu
50Hz (324MHz/4/1620000) generated from event clock in EVG, done by Guanglei Xu
Interlock design – using UNIV-TTL-IN
Challenges

• Interlock realization
• Synchronized timing
• Timestamp distribution by timing system to control system
Thank you all for your attention.

Reference (documents, discussions)

1. China Spallation Neutron Source, Jei Wei, etc.
2. Front End, Ouyang Huafu, 2007/5/1
3. Linac LLRF, Li Jian, etc.
4. Injection and Extraction, Tang Jingyu, Chi Yunong, Shen Li, etc.
5. CSNS Beam Diagnostics, Xu Taoguangu
6. Discussions with Wang Sheng, Zhang Jing, etc.
7. EPICS Collaboration Meeting, ANL, Argonne, Jukka Pietarinen, Micro-Research Finland Oy.