Candidates to get worth position resolution

1. BPF, ADC input circuit may operate in non-linear region.

2. Tails of BPF output spectrum exceeds Nyquist window (250-375MHz) and it makes folding noise.

3. Triple harmonic (900MHz) also may cause folding noise.

4. Analogue noise from DC-DC converter etc. introduces GND wobble, EMI and so forth.
Block diagram

Overview

Analogue Frontend

Gain: 32.5dB (confirmed)
Max Output: +12dBm (2.5Vpp)

*These tests presented in this slide have been performed with Pre:8dB, Post:0dB setting. Total BPF gain is +24.5dB(x16.8).
ADC input circuit

- 250MHz 300MHz (fs)
- 250MHz 300MHz (fs)
22pF -> Snubber circuit

- Thanks to Adrew’s suggestion and modification, we have achieved +10dB at ADC input with this snubber circuit than 22pF, which also prevents ADC malfunction.

Snubber circuit

Figure 52. Differential Transformer-Coupled Configuration for IF Applications from 150 MHz to 300 MHz

From ADC9467 Datasheet
22pF (before modification)

- HSPICE simulation
  - Gain: 1/3 (-10dB) at 300MHz.
  - Lower capacitance behaves unstable, so cannot reduce its capacitance.
Snubber circuit (after modification)

- HSPICE simulation
  - Almost no gain drop at 300MHz.
  - Implement on ch1, ch2 on #2 board.
ADC output

- Consistent with calculation. x3 gain (+10dB).
- Proved it also suppress the ADC malfunction.
Block diagram of 1kV pulsar test

1kV Pulsar → 40dB Att. → variable Att.x2 (0-70dB, 0-11dB) → 1:2 → 1:2 → BPM Readout (Pre: 8dB, Post: 0dB)

Diagram shows a waveform with peaks and troughs, indicating the output of the pulsar test.
Linearity check (1)

- Attenuator output shows good linearity from 40dB to 0dB.
- BPF output shows good linearity up to 2.85V(10dB) [Spec.2.5Vpp], but after that it shows non-linear behavior. Also lower part of waveform has distortion.

![Graph showing voltage vs. input attenuation]

- 4.8V(Att.:0dB) corresponds to the BPM output at 1nC.
ADC input circuitry

-4dB IL: -0.4dB +6dB

ADCLO CK LVPECL +/- 250MHz

ADL5562
Po1dB=4.9Vpp
(1dB compression point)
-> corresponding input level is 2.46Vpp (11.8dBm).

Acceptable input power:
11.8dBm+4dB+0.4dB=16.2dBm (4.08Vpp)
Linearity check (2)

• Semi-Log plot of ADC output peak-peak difference v.s. Attenuator setting.
  - Observed ADC over level at 10dB setting for ch1, ch2 at lower limit (ADC reading is 0).
  - At 0-5dB, ch3 and ch4 have been saturated.
  - In this setting, >10dB attenuator setting is required to keep linearity.
Linearity check (2)

- To check it more precisely, integration of ADC reading (same manner to calculate position resolution) v.s. attenuator setting is shown.
- Also at lower than 10dB, it seems saturation.
Folding noise at ADC

- Tails over the Nyquist window (250MHz - 375MHz) become folding noise.
Frequency response of the Band Pass Filter (S21)

- 250MHz
- 375MHz
Frequency response of the Band Pass Filter (S21)

300MHz
900MHz
Double Pulse test

- To test in more realistic conditions, two bunch signal is emulated by combining 100ns (20m) delayed and 2ns delayed signal. 50 events has been taken with this setting.
  - Att. Pre: 8dB, Post: 0dB, 40dB+ Additional: 20dB
  - Data: ~ryo/vxworks/work/data/2013June19_exPulsar1kV_no2_doubled/

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<thead>
<tr>
<th></th>
<th>1st</th>
<th>2nd</th>
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<tbody>
<tr>
<td>ch1, 2(X)</td>
<td>12.2um</td>
<td>13.6um</td>
</tr>
<tr>
<td>ch3, 4(Y)</td>
<td>9.5um</td>
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Harmonics (600, 900MHz) reduction with external LPF

• When 300MHz CW input, double harmonic (600MHz), triple harmonic (900MHz) were observed at about -15dB down to the fundamental.

• When LPF (Mini Circuit VLFX-300) is inserted at BPF output, harmonics have been suppressed to almost the BG level (>53dB suppression). In this setting 100 events data were taken.
  – Att. Pre:8dB, Post:0dB, 40dB+ Additional: 20dB
  – Data: ~ryo/vxworks/work/data/2013June20_exPulsar1kV_no1/

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<tbody>
<tr>
<td>ch1, 2(X)</td>
<td>11.9um</td>
<td>14.4um</td>
</tr>
<tr>
<td>ch3, 4(Y)</td>
<td>9.8um</td>
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• No significant difference were observed.
Beam Test

• As we can get about 10um position resolution constantly with pulsar, we confirmed it with beam signal.

• Beam signal were divided to two input signal to emulate ideal (no beam position jitter) beam signal.
Beam Test (cont’d)

• 300 events data were taken.
  – @3-2, PFE 5Hz, 0.3nC
  – Att. Pre:8dB, Post:0dB <= Set this value to keep input <3Vpp.
  – Data: ~/ryo/vxworks/work/data/2013June19_beam_ch12fanout_doubled_ch34_fanout/

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<tbody>
<tr>
<td>ch1, 2(X)</td>
<td>11.9um</td>
<td>14.4um</td>
</tr>
<tr>
<td>ch3, 4(Y)</td>
<td>9.8um</td>
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• At previous test (May 29th):
  – @3-2, PFE 1Hz, 0.5nC
  – Att. Pre:0dB, Post:0dB single pulse
  – Data: ~/ryo/vxworks/work/data/2013May29_beam_ch12fanout_ch34fanout/

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<tr>
<td>ch1, 2(X)</td>
<td>53.8um</td>
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<tr>
<td>ch3, 4(Y)</td>
<td>30.7um</td>
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• Confirmed that the worse position resolution were caused by input saturation.
Beam test (cont’d)

2013June19 @3-2 run1 X
nameh1
Entries 300
Mean 192.5
RMS 9.146
Underflow 0
Overflow 0

2013June19 @3-2 run1 Y
nameh2
Entries 300
Mean -7.778
RMS 13.22
Underflow 0
Overflow 0
Beam Test (cont’d)

• 100 events were taken with 0.45nC.
  – Att. Pre:8dB, Post:0dB, 40dB+ Additional: 20dB
  – Data:
    ~ryo/vxworks/work/data/2013June19_beam_ch12fanout_doubled_ch34_fanout-no2/
  – Event#59 were rejected from analysis because it contains ADC malfunction.

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<tbody>
<tr>
<td>ch1, 2(X)</td>
<td>5.7um</td>
<td>8.2um</td>
</tr>
<tr>
<td>ch3, 4(Y)</td>
<td>5.1um</td>
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• Better position resolution than 0.3nC. Position resolution may be limited by signal source S/N. (i.e. 1kV pulsar might have not a good S/N than high charge beam.)
#59 event data

- Suddenly waveform sign were inverted after time > 288
- Have to check ADC clock delay IC.