Chapter 1

Introduction to the VME64 Extensions Standard

1.1 VME64 Extension Objectives

This standard documents features that can be added to VME64 boards, backplanes and subracks defined in the VME64 Standard.

The following new features are defined for optional usage in VME64x based applications:

- Addition of z & d rows to P1/J1 and P2/J2 connectors
  - With associated pin assignments
- A 2 mm hard metric P0/J0 connector (area) between P1/J1 and P2/J2 connectors
  - With 95 user defined signal pins and 19 or 38 ground pins
- 35 more signal ground return pins in the P1/J1 and P2/J2 connectors
- +3.3 volt power
- Auxiliary power voltage
- 3 more +5V power pins via the 3 VPC power pins
- Slot geographical addressing
- 12 reserved bused signal lines, plus 2 unbused pins for future expansion
- 46 more user defined pins on the P2/J2 connector
- Pins allocated for a test and maintenance bus (T&Mbus)
- 3 mate first-break-last precharge voltage pins for hot swap applications
  - 2 pins are on the P1/J1 connector and 1 pin on the P2/J2 connector
  - Can also be used for +5V power when board is locked into position
  - Required for hot swap applications
- 3 mate first-break-last precharge ground pins for hot swap applications
  - 2 pins are on the P1/J1 connector and 1 pin on the P2/J2 connector
  - Required for hot swap applications
- 2 reserved pins for individual slot power control for hot swap applications
- Front panel EMC protection
- ESD protection
- Solder side covers for hot swap and ESD protection
- Injector/Extractor handles with optional locking feature
- Board slot keying
- Multifunction alignment pin
- Front panel safety ground
- Reserved area on front panel for ID and bar code labels
- Rear I/O transition boards
- Added CR/CSR definition
- A 2eVME protocol that doubles the theoretical peak data transfer rate to 160 MB/sec

1.1.1 VME64 Extensions and VME64x Usage

The phrase "VME64 Extension" has been shortened to VME64x, where "x" implies the "Extensions" word. In product data sheets, user manuals, advertising and other promotional literature, it is encouraged that only these two phrases be used when referencing this standard.

1.1.2 9U Boards, Backplanes and Subracks

9U VME, VME64 and VME64x boards, backplanes and subracks will not be referenced in this standard. Another VSO standard, ANSI/VITA 1.3-1997, VME64x 9U x 400mm Format, specifically defines this capability.

1.2 Terminology

See Appendix A for the new terminology specific to the added features described in this standard. Terminology described in the VME64 Standard is not repeated in Appendix A.

1.3 References

The following publications are used in conjunction with this standard. When they are superseded by an approved revision, that revision must apply.

ANSI/VITA 1-1994	VME64 Standard, Approved April 10, 1995
IEC 61076-4-113	2.54 mm 160 pin connectors complementary to IEC 603-2 Style C connectors
IEC 61076-4-101	2 mm Hard Metric Connector
IEEE 1101.2-1992	IEEE Standard for Mechanical Core Specifications for Conduction-Cooled Eurocards
IEEE 1101.10-1996	IEEE Standard for additional Mechanical Specification for Microcomputers using the IEEE 1101.1 Equipment Practice
IEEE 1101.11-1998	IEEE Standard for Rear Plug-In Units for Microcomputers using the IEEE 1101.1 Equipment Practice, and the IEEE 1101.10 additional Mechanical Specifications
IEEE 1149.5-1995	IEEE Standard Module Test and Maintenance Bus
VITA 1.4	VME64x Live Insertion Draft Standard
VITA 1.6	Keying for Conduction Cooled VME64x Draft Standard
VITA 2	Enhanced Transceiver Logic Device Standard

1.3.1 Connector Notes

The 160 pin connector defined in the IEC 61076-4-113 connector specification is an expanded 96 pin connector that is complementary to the IEC 603-2 Style C connector. Rows a, b & c are identical in form, fit and function to the 96 pin IEC 603-2 Style C connectors, used in original VME and VME64 applications. Rows z and d adds 64 pins to the outer shell for a total of 160 pins.

The 160 pin connectors are forward and backward compatible to the 96 pin connectors. Boards with 160 pin connectors will plug into backplanes using 96 pin connectors and boards with 96 pin connectors will plug into backplanes using 160 pin connectors.

IEC 61076-4-101 defines a family of 2 mm Hard Metric (HM) connectors. The P0/J0/RJ0/RP0 connectors defined in Chapter 3 use a Type B 25 position 2 mm connector variant with 19 positions. Each position provides 5 signal pins plus one or two ground pins.

Chapter 2

VME64x Compliance

2.1 Introduction

In order for VME64x boards and VME64x backplanes to be labeled as VME64x Compliant, they are to incorporate a minimum set of functional features. This chapter specifies that minimum set of features for 3U and 6U boards and backplanes.

Each of these features are described and documented in subsequent chapters within this standard.

2.2 Requirements

Rule 2.1:
To claim compliance to this standard, a product shall also comply to all the appropriate rules in ANSI/VITA 1-1994 VME64 Standard.

Rule 2.2:
In the event of any conflicts between this standard and a referenced standard or specification, this standard shall take precedence.

2.2.1 6U VME64x Board's Minimum Features

Rule 2.3:
In order to be labeled as a VME64x compliant board, the 6U board shall incorporate the following minimum functional features:

- Use the IEC 61076-4-113 160 pin connectors for both the P1 and P2 connectors
- Connect all assigned connector ground pins in rows z, a, b, and c to the board's ground plane (row d ground pins are optional)

Observation 2.1:
All the other features defined in this standard are optional.

2.2.2 3U VME64x Board's Minimum Features

Rule 2.4:
In order to be labeled as a VME64x compliant board, the 3U board shall incorporate the following minimum functional features:

- Use the IEC 61076-4-113 160 pin connector for the P1 connector
- Connect all assigned connector ground pins in rows z, a, b, and c to the board's ground plane

Observation 2.2:
All the other features defined in this standard are optional.

2.2.3 6U VME64x Backplane's Minimum Features

Rule 2.5:
In order to be labeled as a VME64x compliant backplane, the 6U backplane shall incorporate the following minimum functional features:

- Monolithic PCB
- Use the IEC 61076-4-113 160 pin connectors for both the J1 and J2 connectors, with properly defined pin tail lengths

- Connect all assigned connector ground pins in all rows to the backplane's ground plane
- Connect the geographical address pins as defined in this standard
- Route and terminate all defined VME64 and VME64x bused signal lines
- Provide power connection and distribution for +5V, +3.3V, +12V, -12V, +V1, +V2, -V1, -V2, VPC and +5V STDBY.
- If rear I/O is to be used on a backplane, rear connector(s) are designed per IEEE 1101.11 for support of rear I/O transition boards.

Observation 2.3:

All the other features defined in this standard are optional.

2.2.4 3U VME64x Backplane's Minimum Features

Rule 2.6:

In order to be labeled as a VME64x compliant backplane, the 3U backplane shall incorporate the following minimum functional features:

- Use the IEC 61076-4-113 160 pin connector for the J1 connector, with properly defined pin tail lengths
- Connect all assigned connector ground pins in all rows to the backplane's ground plane
- Connect the geographical address pins as defined in this standard
- Route and terminate all defined VME64 and VME64x bused signal lines
- Provide power connection and distribution for +5V, +3.3V, +12V, -12V, +V1, +V2, -V1, -V2, VPC and +5V STDBY.

Observation 2.4:

All the other features defined in this standard are optional.

Chapter 3

P1/J1 & P2/J2 160 Pin Connectors

3.1 Introduction

This chapter specifies the usage (beyond the VME64 Standard) of a 160 pin connector for both the P1/J1 and P2/J2 connector pairs. The 160 pin connector adds two 32 pin rows over the 96 pin (3 X 32) VME and VME64 connectors. The pin definitions for these added rows are defined in this chapter. This 160 pin connector pair is defined in the IEC 61076-4-113 Standard.

These added rows are called the "z" row and "d" row. The z row is adjacent to the a row and the d row is adjacent the c row. The five rows are labeled z, a, b, c and d. Mechanical placement of the 160 pin connectors on VME64x boards and on the VME64x backplanes is defined in IEEE 1101.10.

Each 160 pin connector provides 4 pins that mate-first-break-last (MFBL). The four MFBL pins are d1, d2, d31 and d32. On the P1/J1 connectors all 4 pins are used for hot swap and on the P2/J2 connector, only the lower 2 pins are used for hot swap. Three of these MFBL pins also available for additional +5V power.

3.2 Requirements

3.2.1 160 Pin Connector Placement

Rule 3.1:
VME64x boards shall use the IEC 61076-4-113 160 pin plug connectors for the P1 and P2 connector positions, with a minimum endurance level of 400 mating cycles, which is in accordance to IEC 61076-4-113 performance level 2.

Rule 3.2:
Placement of the P1 and P2 connectors on VME64x boards shall be per IEEE 1101.10.

Rule 3.3:
VME64x backplanes shall use the IEC 61076-4-113 160 pin receptacle connectors for the J1 and J2 connector positions, with a minimum endurance level of 400 mating cycles, which is in accordance to IEC 61076-4-113 performance level 2.

Rule 3.4:
Placement of the J1 and J2 connectors on VME64x backplanes shall be per IEEE 1101.10.

Permission 3.1:
Selective loading only the signal and power pins in the P1 and P2 connectors may be used on VME64x boards.

Rule 3.5:
The ground pins shall always be loaded in the P1 and P2.

Rule 3.6:
All pins in the J1 and J2 connector shall always be loaded.

Observation 3.1:
In some applications, not all pins are needed (used) in the P1 and P2 connectors. Using selectively loaded connectors could provide a cost savings and will reduce insertion/withdrawal forces.

3.2.2 P1/J1& P2/J2 Connectors, Rows z & d Pin Assignments

Rule 3.7:
The signal pin assignment of the P1/J1 and P2/J2 connector pairs, rows z and d shall

be as defined in Table 3-1, P1/J1 and P2/J2 Rows z & d Pin Assignments. See Appendix B for definition of these signals.

Table 3-1 P1/J1 and P2/J2 Rows z & d Pin Assignments

Position No.	P1/ J1		P2/ J2	
	Row z	Row d	Row z	Row d
1	MPR	VPC (1)	UD	UD (1)
2	GND	GND (1)	GND	UD (1)
3	MCLK	+V1	UD	UD
4	GND	+V2	GND	UD
5	MSD	RsvU	UD	UD
6	GND	-V1	GND	UD
7	MMD	-V2	UD	UD
8	GND	RsvU	GND	UD
9	MCTL	GAP*	UD	UD
10	GND	GA0*	GND	UD
11	RESP*	GA1*	UD	UD
12	GND	+3.3V	GND	UD
13	RsvBus	GA2*	UD	UD
14	GND	+3.3V	GND	UD
15	RsvBus	GA3*	UD	UD
16	GND	+3.3V	GND	UD
17	RsvBus	GA4*	UD	UD
18	GND	+3.3V	GND	UD
19	RsvBus	RsvBus	UD	UD
20	GND	+3.3V	GND	UD
21	RsvBus	RsvBus	UD	UD
22	GND	+3.3V	GND	UD
23	RsvBus	RsvBus	UD	UD
24	GND	+3.3V	GND	UD
25	RsvBus	RsvBus	UD	UD
26	GND	+3.3V	GND	UD
27	RsvBus	LI/I*	UD	UD
28	GND	+3.3V	GND	UD
29	RsvBus	LI/O*	UD	UD
30	GND	+3.3V	GND	UD
31	RsvBus	GND (1)	UD	GND (1)
32	GND	VPC (1)	GND	VPC (1)

Note: (1) These pins are MFBL (mate-first-break-last) pins

Observation 3.2:

Pins d1 and d2 of the P2 connector will mate before the other pins in rows z, a, b, c and d. Be aware that this could cause problems with user defined I/O signals when these pins mate before the other I/O pins during live insertion operations.

Recommendation 3.1:
Be aware that during live insertion operations, the VPC power could be applied first, therefore boards should be designed to tolerate the application of VPC before GND is connected. The same applies during live removal, where VPC could be the last contact to be removed.

Observation 3.3:
Specification of the +3.3V, +V (+V1 & +V2) & -V (-V1 & -V2) [Auxiliary] and VPC power are defined in Sections 3.2.4, 3.2.5 and 3.2.6 of this standard.

Rule 3.8:
The GND pins shall be connected to the VME64x board's signal ground plane and the VME64x backplane's signal ground plane.

Rule 3.9:
The UD, User Defined, pins shall be treated in the same fashion and have the same rules as the User Defined pins in the VME64 Standard.

Rule 3.10:
The RsvBus (reserved bused) pins shall not be used by VME64x boards and are reserved for future use.

Rule 3.11:
The 14 RsvBus pins, the 5 test and maintenance bus (MPR, MCLK, MSD, MMD & MCTL) pins and the RESP* pin shall be bused and terminated on VME64x backplanes that implement a 160 pin connector for J1 in the same fashion and have the same rules as the other VME64 bused signals defined in the VME64 Standard.

Rule 3.12:
The LI/I* (Live Insertion/Input) and LI/O* (Live Insertion/Output) pins shall be reserved for specification by the VITA 1.4-199x VME64x Live Insertion Draft Standard.

Observation 3.4:
The LI/I*, LI/O* and RsvU pins are not bused but just feed through the backplane.

Rule 3.13:
The five test and maintenance bus signal lines (MPR, MCLK, MSD, MMD & MCTL) shall be reserved for specification by the IEEE 1149.5 MTM-Bus Standard.

Rule 3.14:
The ground (GND) return path on the backplane shall present a maximum peak to peak voltage differential of 50 mV across the backplane, measured between any connector pin making contact with the GND rail, under conditions of maximum current demand and all conditions of loading and noise expected for that system. Backplane termination networks are included in this rule. This applies for all frequencies, including DC.

Rule 3.15:
A voltage differential no greater than 50 mV shall be presented across the +5V, +3.3V, +12V and -12V power rails and 200 mV across the +V and -V power rails, when measured between any two connector pins making contact with the respective power rail, under conditions of maximum current demand and all conditions of loading and noise expected for that system. This applies for all frequencies, including DC.

Observation 3.5:
While VME64x boards (with 160 pin connectors) can physically be plugged into a VME64 backplane (with 96 pin connectors), the two outer rows of pins, z and d, will not be connected to anything.

Recommendation 3.2:
Given Observation 3.5, the user should determine from the vendor whether a specific VME64x compatible board can be configured to operate correctly in a VME64 backplane.

Permission 3.2:
Vendors may design VME64x boards that can only be used in VME64x backplanes.

3.2.3 Geographical Address Pin Assignments

Rule 3.16:

The 6 geographical address pins (GA0*, GA1*, GA2*, GA3*, GA4* and GAP*) shall be tied to ground or left open (floating) on the backplane J1 connector as defined in Table 3-2, Geographical Address Pin Assignments.

Table 3-2 Geographical Address Pin Assignments

Slot No.	GAP* Pin	GA4* Pin	GA3* Pin	GA2* Pin	GA1* Pin	GA0* Pin
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21.	Open	GND	Open	GND	Open	GND

Observation 3.6:

Boards which use the geographical address signals will most likely use a pull up resistor to Vcc. The device that samples the levels of the geographical address pins will read the inverted value of the slot number into which the board is plugged. When the board is plugged into a VME/VME64 backplane the slot number will be zero with a parity error (GAP* open).

Rule 3.17:

The board shall limit the current through each geographical address pin to a maximum of 2 mA.

3.2.4 +3.3V Power

Rule 3.18:

The +3.3V power supplied to each slot on the VME64x backplane shall remain within

the limits of +3.25V to +3.45V, including regulation variation, noise and ripple frequencies to 20 MHz.

Rule 3.19:
The current drawn for +3.3V pins shall follow the maximum current draw per power pin as specified in the VME64 Standard, Figure 5-7, Current Rating For Power Pins.

Observation 3.7:
If the maximum board ambient temperature is 60° C, the maximum current that can be drawn per power pin in a multi-pin configuration is 1.25 Amp. With 10 +3.3V power pins on the P1/J1 connector pair, a nominal 41 watts of +3.3V power can be supplied to a VME64x board.

Rule 3.20:
+3.3V, +5V, +12V, -12V and Auxiliary power will ramp up and down independently of one another. Boards shall be designed to accommodate any combination of power up and down sequence without causing board failure.

3.2.5 V1/V2 Auxiliary Power

Rule 3.21:
The V1/V2 auxiliary power supplied to each slot via the +V1, +V2, -V1 and -V2 power pins on the VME64x backplanes shall remain within the limits of 38V to 75V, including regulation variation, noise and ripple frequencies to 20 MHz.

Rule 3.22:
The current drawn for the +V1, +V2, -V1 and -V2 pins shall follow the maximum current draw per power pin specified in the VME64 Standard, Figure 5-7, Current Rating For Power Pins.

Rule 3.23:
Each board's power draw of the V1/V2 power shall be balanced between the +V1 plus +V2 and -V1 plus -V2 power pins, with no more than 1 mA of current going through the ground pins.

Recommendation 3.3:
The V1/V2 leakage current should be kept below 100 uA.

Rule 3.24:
The system auxiliary power supply of the V1/V2 power shall ensure that the +V1 and +V2 voltages are always above or equal to the ground voltage level and that the -V1 and -V2 voltages are always below or equal to the ground voltage level.

Observation 3.8:
If the +V1 and +V2 voltage rails are tied to ground and the +12V power is used, the nominal voltage between the +12V and the -V1 and -V2 power rails is 60 volts. With voltage tolerances, the 60 volt maximum is exceeded. Additional protection might be needed to comply with local and national regulatory agencies.

Recommendation 3.4:
System implementors and users should be aware that the United States Underwriters Laboratory (UL) rules that whenever any two power points within a system (black box) exceeds 60 V, it is considered unsafe for "human operation". The design of boards will allow for larger voltages between any combination of power rails. But, how a "VME64x System" is integrated is the responsibility of the system integrator, and should comply with all applicable laws and regulations with respect to safety and other computer requirements, including EMC.

Observation 3.9:
For some applications, dual V1/V2 power rails are required. It might be necessary to build backplanes that split the +V1 and +V2 into two power rails, and/or split the -V1 and -V2 into two power rails.

Recommendation 3.5:

The usage of single or dual V1/V2 supply and the decision whether the negative or the positive poles will be tied together, is up to the system configuration. Generic VME64x backplanes should provide individual connections for each of the +V1, +V2, -V1, -V2 power rails.

Rule 3.25:

Boards that use the dual V1/V2 power rails shall place diodes or equivalent on each of +V1 and +V2 power lines and on each of the -V1 and -V2 power lines. In event one of the V1/V2 power rails fails, the other power rail will supply the auxiliary power to the board.

3.2.6 VPC Power and Additional +5V Power

VPC is collectively the three pre-charge voltage pins on the P1/J1 and P2/J2 connectors. These three pins mate a minimum of 1.5 mm before the other pins during live insertion. During live withdraw, these pins are the last to break contact. This feature is required to support the hot swap capability defined in the VITA 1.4-199x VME64x Live Insertion Draft Standard.

Rule 3.26:

If VPC power is used, all three VPC power pins shall be used on 6U boards and both VPC power pins on 3U boards shall be used.

Rule 3.27:

The VPC voltage pins shall be connected directly to the backplane +5V power plane.

Observation 3.10:

Boards used for hot swap need to limit the peak current drawn through each of the VPC power pins during connector mating and disconnect operations. The current limit is defined by the VITA 1.4-199x VME64x Live Insertion Draft Standard.

Permission 3.3:

VPC power pins may be used for additional +5V power when fully plugged in and locked into position.

Rule 3.28:

If the VPC power pins are used for additional +5V power, the current drawn shall follow the maximum current draw per power pin as specified in the VME64 Standard, Figure 5-7, Current Rating For Power Pins.

Observation 3.11:

If VPC power is shorted to +5V power on a board, the board can't be used in hot swap applications.

3.2.7 Reset and ACFail

Rule 3.29:

If +3.3V and/or Auxiliary power is used to power boards plugged into the backplane, the SYSRESET* and ACFAIL* signals operations levels shall include the proper functional levels of +3.3V and Auxiliary.

Observation 3.12:

Rule 3.29 implies that the SYSRESET* and ACFAIL* signal lines can not be released high (normal operation) until the monitored power voltages are in the proper operation levels. When any of the power signals goes outside the proper operation range, the SYSRESET* signal line is asserted. The timing of these two signals remains the same as defined in the VME64 Standard.

3.2.8 Board Power Dissipation

Recommendation 3.6:

Board suppliers should specify a board's maximum power dissipation and identify "hot

spots" and any thermally sensitive components, which require higher cooling airflow than normal.

3.2.9 Backplane Termination Network using +3.3V Supply

Permission 3.4:

The +3.3V supply voltage may be used for the backplane termination network's power.

Rule 3.30:

If the +3.3V supply voltage is used for the backplane termination network, the network shall be in compliance with the network shown in Figure 3-1 Backplane Termination Network using +3.3V Power.

Recommendation 3.7:

For VME64x backplanes that use +3.3V power for the termination network, a large warning label should be attached to the back side of the backplane stating that the termination network is supplied by the +3.3V power rails. "+3.3V power is required for proper VME64x system operation."

Observation 3.13:

The backplane voltage tolerance is better than required for the +3.3 V termination network.

3.2.10 Monolithic Backplanes

Rule 3.31:

6U VME64x backplanes shall be constructed as a single (monolithic) printed circuit board.

Observation 3.14:

The main reason for Rule 3.31 is to provide solid voltage and ground planes on the backplane to minimize the noise and voltage differentials between VME64x boards and VME64x backplanes.

3.2.11 Geographical Address Implementation

This section ties together the implementation of geographical addressing and CR/CSRs if both are implemented on a VME64x board.

Geographical addressing as defined in Section 2.2.3 is to be used by VME64x boards to automatically identify into which VME64x backplane slot it is plugged. Based on that information, software can automatically configure the boards for slot specific functionality. Initialization and configuration of the CR/CSRs is an extension of the capability.

The monarch is generally the first CPU board to gain access to the backplane and system right after power up to configure the system. The monarch might also be the CPU board which controls and manages the main system operation during normal operations.

Rule 3.32:

If a board implements both geographical addressing and CR/CSR capability, the BAR value shall be derived from the geographical address pins.

Observation 3.15:

The above rule will automatically place each board's CR/CSR address in the proper A24 address space. This will allow the system's monarch to search the CR/CSR address space and quickly determine which VME64x boards are plugged into the backplane and then configure the board.

Recommendation 3.8:

Boards implementing Rule 3.32 should parity check the geographical address. If bad parity is found, the local address should be set to decimal 30 (Ox1E) (the amnesia address).

Permission 3.5:

If bad geographical address parity is detected the board may not respond to CR/CSR accesses from the bus.

Observation 3.16:

It is up to the system designer to determine how to handle multiple occurrence of geographical parity errors, if multiple parity errors do occur.

Rule 3.33:

Monarchs that search the CR/CSRs space for presence of VME64x boards shall also look for boards at amnesia address 30 (Ox1E) and take the appropriate action if one is found at that address.

Permission 3.6:

VME64x boards that need to be backward compatible to original VME backplanes, may add some sense circuitry and 5 switches or 5 jumpers or some programmable logic. When the board senses that none of the GA*[4..0] lines are tied to ground (board not plugged into a VME64x backplane), it will use the state of the 5 switches or 5 jumpers or programmable logic values for the geographical address value.

Observation 3.17:

The BAR bits 7 to 3 defined in the CR/CSR regions, correspond to A[23..19] in the CR/CSR space. See Table 2-31 and Section 2.3.12 in the VME64 Standard for more explanation.

3.2.12 Connector Tail Lengths

Recommendation 3.9:

All backplane J1 and J2 connector tail pins that are connected to bus signal lines should be of the short length, 5 mm or less.

Rule 3.34:

If backplane application is intended to support rear I/O transition boards, then the J2 B row of power and ground pins shall be 17 mm in length.

Observation 3.18:

Recommendation 3.9 provides protection of the electrical properties of all bused signal lines on the backplane.

Rule 3.35:

When straight through I/O is used, a shroud over the rear long tail pins shall be used that meets the mechanical dimensions defined in IEEE P1101.11.

3.2.13 Labels on 96-pin Plug Connectors

Rule 3.36:

All VME64 and VME64x boards that utilize the 96-pin plug connector shall not place labels or any other markings on the outer shroud.

Observation 3.19:

When 96-pin plug connectors are plugged in to a 160-pin receptacle connector, the two outer contact rows contact directly on the outer shroud. Any added material will cause the board's insertion forces to be higher as well as will rub off the labels or any other marking material.

3.2.14 Backplane Connectors with Keying Devices

Observation 3.20:

Some VME boards and backplanes use 96-pin connectors with a built in keying device. A VME64x board with a 160-pin connector cannot be plugged into such a backplane. The outer rows of the 160-pin connector will be blocked by the keying device, preventing the two connectors from mating.

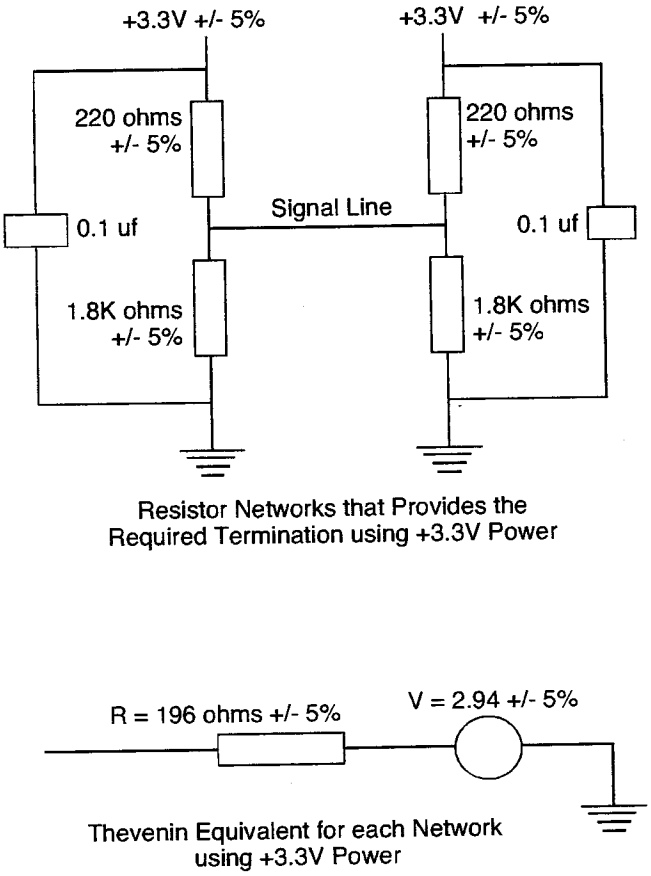

Figure 3-1 Backplane Termination Network using +3.3V Power