OPTICALLY COUPLED FDC-DFC MODULE

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ABSTRACT

A new module has been developed to improve a computer controlled analog-light-link system. The module has frequency synthesizers, frequency counters, optical transmitters and optical receivers in it. Accuracy, reliability and maintenability of the system were greatly improved by the module.

INTRODUCTION

In an accelerator system, especially in ion sources, signals are exchanged between devices at different potentials. We have four ion sources in the negative ion injector for the JAERI tandem accelerator. The ion sources are controlled with a CAMAC crate on the high voltage deck. To send control voltage signals, voltage to frequency conversion(VFC) and frequency to voltage conversion(FVC) technics were used and the frequency was transmitted with optical fiber links. This technic is traditional and easy to accomplish high voltage isolation. Figure 1a shows the analog light link system which was used in the tandem. DAC and ADC modules were used for output and input of analog voltage, respectively. Surge protection modules were used to protect CAMAC modules against external surges. The system was less reliable and had poor accuracy.

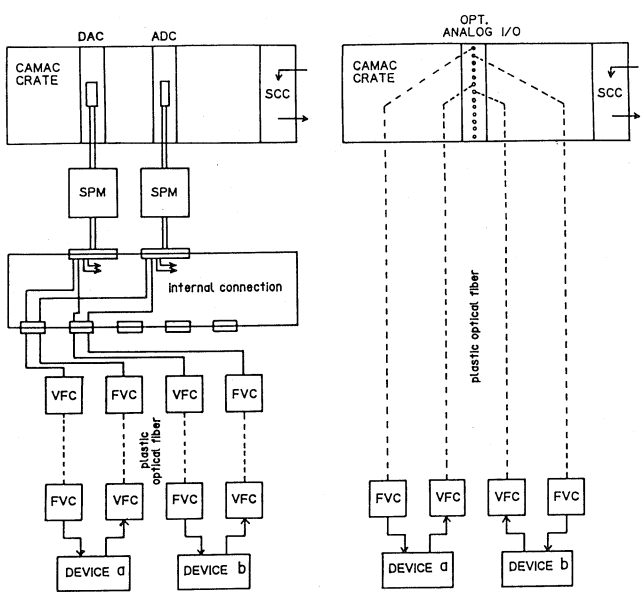

Figure 1a Figure 1b

Figure 1. Block Diagram of an Analog Light Link. Figure 1a and 1b correspond to the old system and the new system, respectively.
SCC : Serial Crate Controller
SPM : Surge Protection Module
VFC : Voltage to Frequency Converter
FVC : Frequency to Voltage Converter
OPT. ANALOG I/O : Optically Coupled FDC-DFC Module

While we had a plan of extending the injector, we decided to revise the system. For the purpose, we develop a new module, with which the ADC, the DAC and the surge protection modules were replaced. It is an interface device between CAMAC dataway and optical signals in the above light link. Thus it is called optically coupled FDC(frequency to digital converter)-DFC(digital to frequency converter) module. Figure 1b shows a block diagram of the new light link system with the module.

COMPOSITION OF THE MODULE

To receive reading value, the module counts flickering frequency of the lights. To send a control value, it generates a frequency signal from a digital value by a frequency synthesizer using phase locked loop(PLL) technic. There is no need to have the intermediate voltage signals between DAC and VFC nor between FVC and ADC. Since the optical fibers are directly connected to the module, the surge protection modules in Fig. 1a can be removed.

The module has 5 control channels and 8 input channels within a single width CAMAC module. These numbers, 5 and 8 channels, were decided to match the control of the ion sources. The specification of the module is designed to have upward compatibility with the old system. Table 1 shows the design specification of the DFC and the FDC. In the old system, signal voltages of 0 V to 10 V were corresponded to frequencies of 1 KHz to 10 KHz.

Figure 2 shows a block diagram of the module. It consists of 5 DFC's, 8 FDC's, a time base, a control logic and a dataway interface.

Table 1

Design specification of DFC and FDC

DFC

setting(N)	output(F)	FVC output
0, 1	2.5 Hz	
400	1 KHz	0 Volt
4000	10 KHz	10 Volt
1≤ N ≤4095	F=2.5 Hz * N	
accuracy	15 ppm(25°C±10°C, 1 year)	

FDC

input(F)	count(N)	VFC input
250 Hz	100	
1 KHz	400	0 Volt
10 KHz	4000	10 Volt
10237.5Hz≧F≧250Hz	F/2.5Hz	
accuracy	±1	
F≧10240KHz	4095	

: FVC output and VFC input are only for references.

OUTPUT CHANNEL

Figure 3 shows a block diagram of one of 5 output channels, DFC's. Data coming from the dataway are loaded into a 12 bit data register. The PLL synthesizes the frequency proportional to the value in the data register. The frequency is divided by 100 and optical transmitter sends it in the form of optical signal. The divider improves a relation between the resolution of frequency setting(2^{-12} of full scale, 2.5 Hz) and response time of the PLL. The sampling frequency of the phase detector in the PLL is 250 Hz(2.5 Hz * 100), and response time of the system is greatly reduced with the same resolution. A low pass filter in the PLL is shown in Fig. 4. The phase detector is the

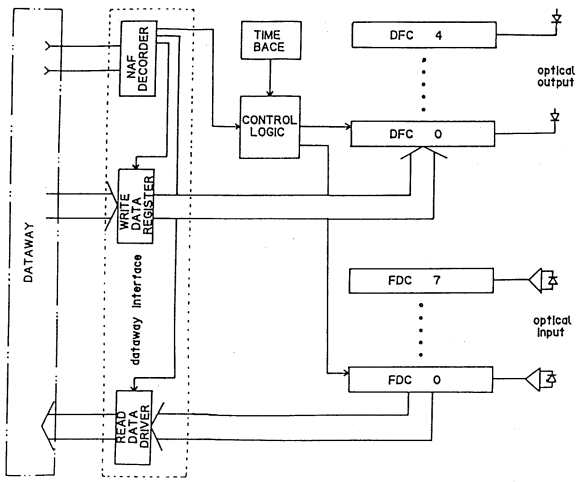

Figure 2. Block Diagram of the Optically coupled FDC-DFC module.
DFC : Digital to Frequency Converter(F/D)
FDC : Frequency to Digital Converter(D/F)

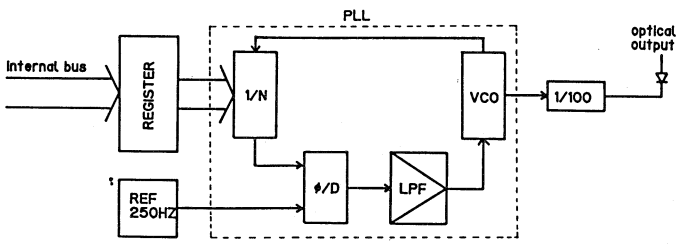

Figure 3. Block Diagram of DFC.
1/N : Programmable Dived by N Counter
φ/D : Phase Detector
LPF : Low Pass Filter
VCO : Voltage Controlled Oscillator

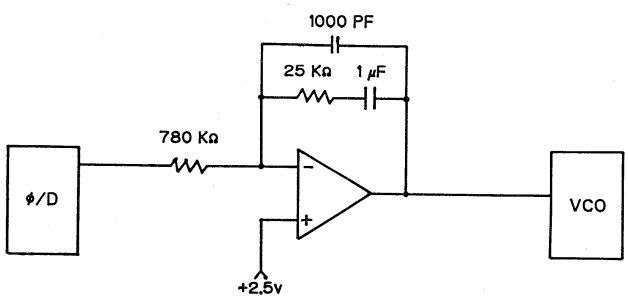

Figure 4. Low Pass Filter of the PLL.

one with charge pump in it.

The PLL limits the response time of the output channel. It takes about 6 seconds to change the output of the DFC from 1 KHz to 10 KHz. Since the PLL monitors the output frequency and keeps the ratio of the output and the time base equal to the stored value in the data register, long term deviation of the output frequency is proportional to the deviation of the time base in a stational state. Fluctuation of the output in a short term depends on noise and remaining ripple of the low-pass filter and a voltage controlled oscillator(VCO) of the PLL. A control logic arbitrates between accesses from the dataway and the PLL to the data register. Thus the output is glitch-free from the dataway cycles.

INPUT CHANNEL

The input channels, FDC's, receive optical signals and count the flickering frequency to load into data registers. Figure 5 shows a block diagram of one of the 8 input channels.

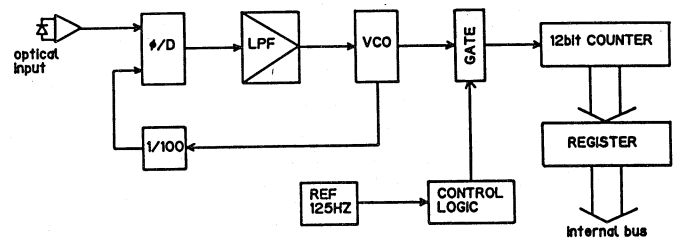

Figure 5. Block Diagram of FDC.
φ/D : Phase Detector
LPF : Low Pass Filter
VCO : Voltage Controlled Oscillator

Similarly to the case of DFC, we want to treat them in a higher frequency. The input frequency is multiplied by 100 with a PLL. Conversion speed is multiplied by 100. In every interval of 1/125 seconds, the pulses of the multiplied frequency in 1/250 seconds are counted and the count is loaded to a data register, which is read through the dataway. Since the FDC digitizes analog quantity, quantization error of 1 LSB(2^{-12}) is inevitable. Error caused by the time base is negligibly smaller than the quantization error.

TIME BASE

The time base is generated from output of the high accuracy quartz oscillator. Its accuracy is ±15 ppm in 25°C±10°C over a year.

REALIZATION OF THE MODULE

Circuit density in the CAMAC crate affects the system cost. Channel density of the module depends on both the numbers of optical transmitters and the optical receivers which can be attached to the front panel of the module and occupied area on the P.C. board of the circuits. Hewlett Packard HFBR-1501's and HFBR-2501's are used as the optical transmitters and the receivers, respectively. Several programmable array logics(PAL's) are used to improve space efficiency and to simplify building blocks. About 120 IC's are mounted on a 4 layered P.C. board and the previously mentioned number of channels are realized in a single width CAMAC module.

The module is designed to have no adjust point. Number of the adjust points in the light link system was reduced to 2/5 of the previous one.

RESULTS AND DISCUSSIONS

The seven modules were made and 4 of them have been used to control the 4 negative ion sources of the injector. There have been no trouble, since the modules were used in the system. Because the module has appropriate numbers of input and output channels in it and receives or transmits optical signals directly, the number of interconnections was reduced between CAMAC crate and the devices around the ion sources. With newly designed FVC and VFC

module, accuracy and reliability of the system is greatly improved. Over all accuracy of the light link system is about 0.3% of full scale and is mainly due to the VFC and the FVC.

ACKNOWLEDGEMENT

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