Phase Monitor with sampling electronics for RCNP Ring Cyclotron

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Abstract

As the new phase monitor for the RCNP Ring Cyclotron, a circuit system with sampling electronics is designed and made.

1 Introduction

The beam phase at the RCNP Ring Cyclotron is monitored by the circuit system with the frequency conversion method. But the information obtained using this method is in principle only the beam phase based the one of the accelerating voltage. To monitor not only the phase information but also the beam shape, the new circuit system with sampling electronics is designed and made.

2 New circuit system for the beam monitor

2.1 *Sampling Concept*

The beam accelerated at AVF Cyclotron is injected to Ring Cyclotron every three or five RF acceleration cycles. Therefore, the output signal originated in the accelerated beam is obtained per 3 or 5 accelerating RF periods. Because of high acceleration voltage, the RF signal is larger than the beam signal. When the beam current is several nA, a typical S/N ratio is about 1/1000. To eliminate the large RF noises from signal of phase probe, and pick out this weak signal, a signal line delayed exactly one RF period based on the other signal line is arranged, and subtract both signals. The sampling system based on the principle is shown in Fig.1. In case (A), input signal is sampled by two different sample and hold circuit. One of the sampling pulse is shifted one RF cycle. Finally, the output signal is acquired from the differential amplifier. In this case, because of effects not only the error originated in delay line but also the ones in each sample and hold circuit, the accuracy is not expected in that situation to deal with the small signal of micro voltage level. As case (B), dealing the signal from single sample and hold circuit, the RF background

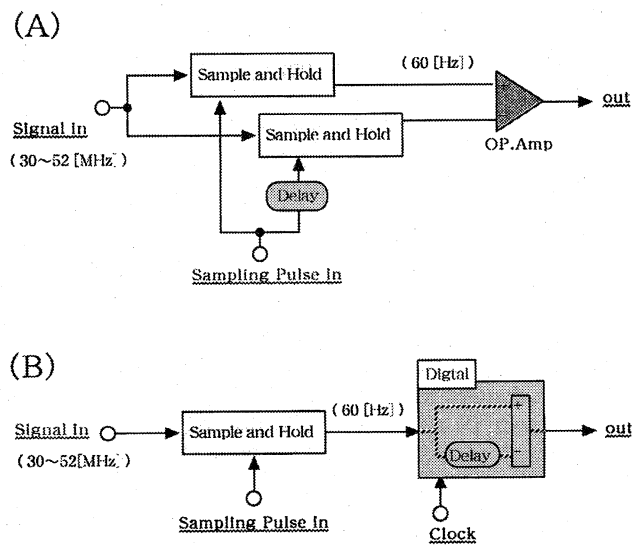

Figure 1: **Sampling concept**

is digitally subtracted. The errors above mentioned are in principle canceled each other.

2.2 *Sampling Electronics*

Fig.2 shows the sampling block diagram designed using the concept (B).

Sample and Hold circuit(Unit① in Fig.2)

The input frequency $\omega_d(30\sim52\mathrm{MHz})$ is converted to $\Delta\omega(60\mathrm{Hz})$ exactly based the sampling method, and is filtered using LPF(Low Pass Filter). The characteristic of the LPF is 36dB/oct, $f_c \simeq 6.4kHz$.

Sampling Pulse generator (Unit②)

The sampling pulse generator can be operated in normal sampling mode or special sampling mode. On the normal sampling mode, the repetition (angular) frequency of the sampling pulse is set on $\frac{1}{n}\omega_s$ $(n \in N)$, and on the special sampling mode, the repetition frequency of the sampling pulse is $\frac{2}{2k-1}\omega_s$ $(k \in N)$. On the latter mode, odd harmonic componens of the RF signal are rejected strongly, and only even ones are sampled [1], [2].

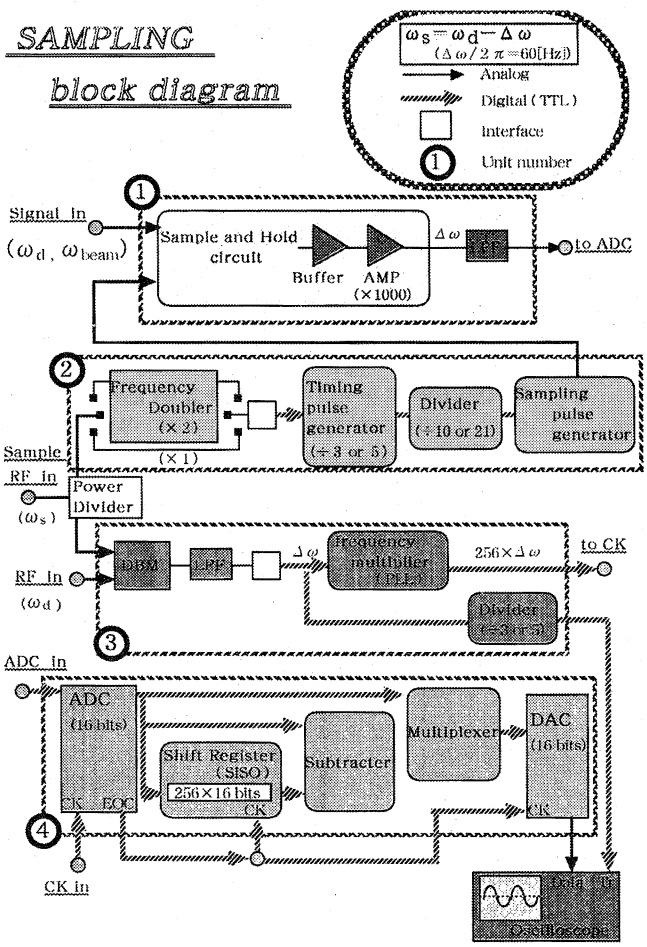

Figure 2: **SAMPLING block diagram**

The sampling timing signal (ω_s) finally generates the sharp sampling pulse. The sampling pulse repetition frequency of this system are $(\frac{1}{10}, \frac{1}{30}, \frac{1}{50}, \frac{2}{21}, \frac{2}{63}, \frac{2}{105}) \times \omega_s$.

Clock and Trigger generator (Unit③)

The sampling timing signal(ω_s) and the RF signal(ω_d) are mixed by a DBM(Double Balanced Mixer) and generates a low frequency signal($\Delta\omega$). The signal is multiplied 256 times exactly at PLL(Phase Locked Loop) and is used to the clock for the digital elements. The frequency is 60 × 256 = 15.36kHz. The signal is also divided properly for a trigger pulse of an oscilloscope to observe the beam signal.

Digital Processing Unit (Unit④)

The maximum input voltage of ADC is adjusted to ± 5V at OP.amp of the Sample and Hold circuit, and the output voltage of this section is ± 11V. While one period of the input frequency($\Delta\omega$=60Hz), the input signal is AD-converted 256 times and the 16 bits digital data is being memorized on the 16 × 256 bits shift register at real time. Finally, the both(input and output of this shift register) data are subtracted and DA-converted after the bits adjustment.

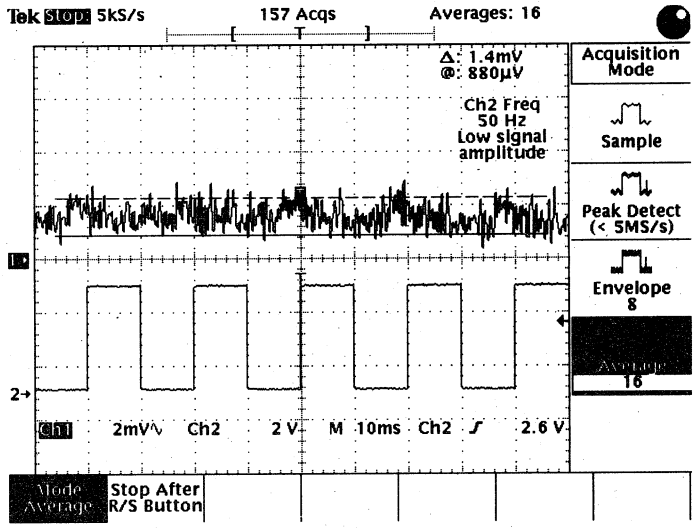

Figure 3: **Digital Processing Circuit Test** Ch1 is the output voltage and Ch2 is the 50Hz trigger pulse. The output voltage is observed with an average mode of the oscilloscope. The averaging is 16 times.

3 Performance Test

This section estimates the noise(RF etc) suppression efficiency of the circuit systems (Unit④ only, and all) in Fig.2.

3.1 *Digital Processing Unit Test*

Fig.3 shows the the noise suppression at Digital Processing circuit only. The input voltage and frequency are a $10V_{p-p}$ sine wave and 50Hz. The extent of the output voltage is about $2mV_{p-p}$. Therefore, the signal originated in orbit particles larger than 1mV can be identified by this method.

3.2 *Overall Test*

Fig.4 shows the the noise suppression at all unit including the sample and hold circuit. The input voltage and frequency $\Delta\omega$ are -40dBm and 60Hz, respectively. The extent of the output voltage is about $220mV_{p-p}$. Therefore, the signal larger than -80dBm is discerned at present.

4 Conclusion

At Digital Processing Circuit Unit only,the noise suppression is about 80dB. At Overall Unit, the suppression is about 40dB at the present condition. Presently, the resolution of this system is being improved and the additional systems are under construction.

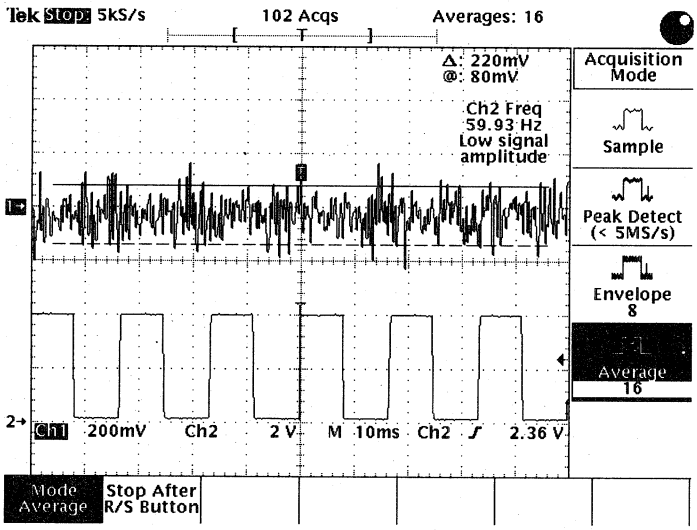

Figure 4: **Overall Test** Ch2 is the 60Hz trigger pulse.

References

[1] J.F.P. Marchand, F. Shutte and H.L. Hagedoorn, Rev. Sci. Instrum., Vol.45, (1974) 361.

[2] T.Saito, H.Tamura, RCNP Annual Report (1980) 172.