An All-Digital Low Level RF System Based On FPGA Technology

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Abstract

An all-digital low level rf system has been designed and constructed for a proton synchrotron for medical application. The system is centered on the RF Controller, a double-width VME board. The Controller handles all the functions of the low level rf system. Its main features include 64MB of on-board DRAM bank to store up to 60 operating patterns, a memory management system to oversee the patterned operation, as well as filtering and feedback of the low level signal, and communication with the VME bus. These functions are realized by two Field Programmable Gate Array (FPGA) chips for fast parallel processing. The design features of the RF Controller and some test results are discussed in this paper.

1 Introduction

It is becoming increasingly popular to incorporate the advances of digital technology into the low level rf systems [1],[2],[3]. Already the Direct Digital Synthesizer (DDS) has become common place, replacing the VCO as the signal generator. Digital processing in such cases are performed by conventional logic gates and hence fixed by hardware. A Digital Signal Processor (DSP) may be included in the system, but its role is often limited to that of passing along patterned data. Although it is useful to have a DSP directly in the phase loop to introduce active and passive filters with time-varying gains, the processing speed at present is limited to about 200 kHz for an updating cycle, even with a dedicated DSP. This therefore has been the bottleneck to having a DSP directly in the phase loop of a moderate to fast cycling synchrotron [2].

In the context of such a limitation, we have selected to implement the feedback loops with FPGA. This solution opens up ways to control the loop parameters in real time by treating them as patterned data. At the same time it provides the flexibility of operation during accelerator commissioning. Since the FPGA is an inherently parallel processor, the entire feedback algorithm can be processed in several clock cycles. The FPGA can be operated at a clock rate of over 100 MHz and an inter-pin delay time of 4.5 ns. The hardware allows for flexibility since the FPGA software can be modified by rewriting the EPROM. The parameters of the feedback loop can also be changed on line.

A unique feature of the RF Controller is that it is controlled solely by the FPGA, including the communication interface to the VME processor. We chose not to include the DSP. This is because the added flexibility is not required for the present application, intended for a hospital-based medical accelerator. Another reason was that the DSP is not used in any other part of our accelerator control system, hence we chose to limit the variety of hardware for maintenance purposes. However, a hybrid DSP/FPGA system may be better suited for a research accelerator in terms of the operational latitude.

2 RF Control System

Figure 1 is a block diagram of the RF control system. The parameters of the medical proton synchrotron are given in table 1. A block diagram of the RF Controller is shown in figure 2 and the parameters are given in table 2.

The RF Controller consists of the following functional blocks.

(1) Data transfer from HP-RT
(2) Memory address management of patterned data
(3) Digital processing of feedback data
(4) Analog electronics for low-level rf

Table 1 Parameters of the medical proton synchrotron

Extracted beam energy	70 - 250 MeV
Injected beam energy	3 MeV
Circumference	19.86 m
Number of particles	1 x 10^{11}
Beam current	19 - 150 mA
Accelerating rf frequency	1.2 - 9.3 MHz
Harmonics	1
Synchrotron frequency	4 - 5.3 kHz

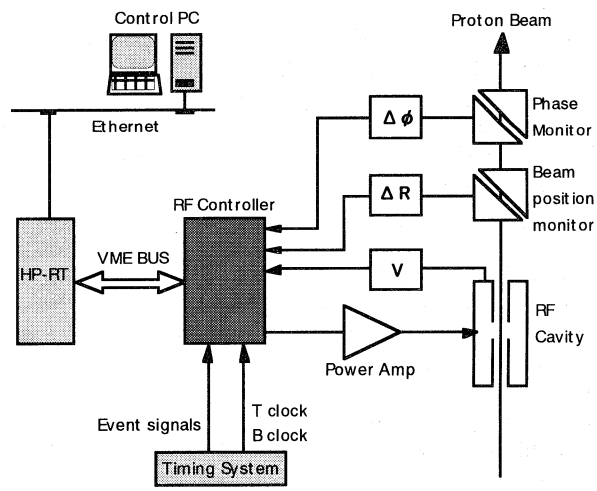

Fig.1 A block diagram of the RF control system.

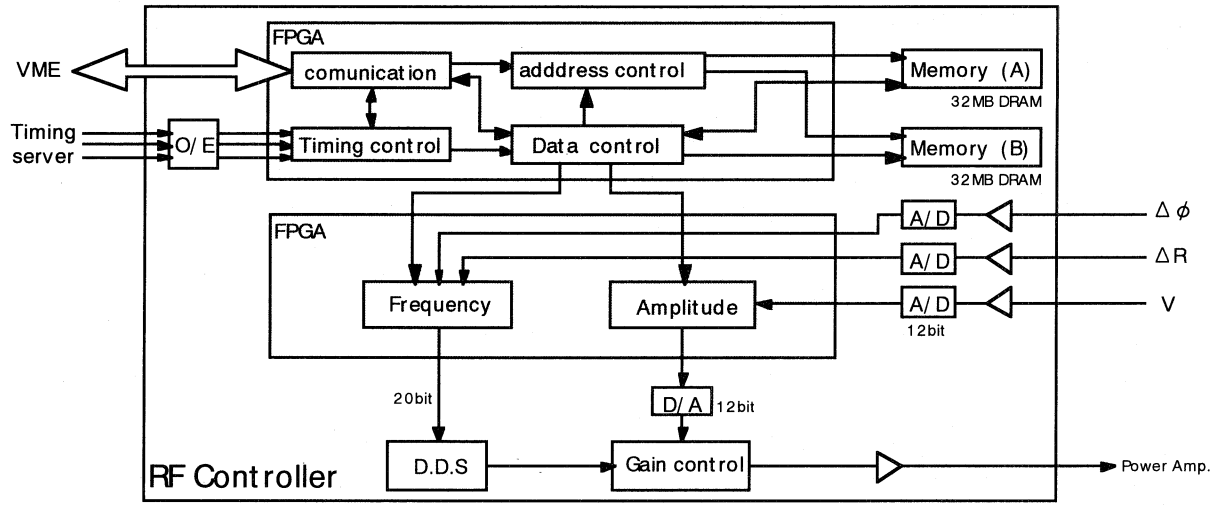

Fig.2 A block diagram of the RF Controller

Table 2 Parameters of the RF Controller

DRAM capacity	64 MB
Number of patterns stored	60
Frequency resolution	20 bits (9.28 Hz)
Accelerating voltage resolution	12 bits (0.25V)
Δ R resolution	12 bits (0.024 mm)
Δ φ resolution	12 bits (0.088 deg)
FPGA clock	10 MHz
ADC/DAC clock	1 MHz
Typical data processing time	1.6 μs

The RF Controller puts out 3 sets of reference pattern data: the rf frequency (20 bits), beam position ΔR (12bits) and rf amplitude (12 bits) for a total of 48 bits/word, including the control field. The frequency and amplitude data are used to set the DDS output which drives a 60 dB power amplifier and a wide-band rf cavity.

There are 3 feedback loops in this system: the Auto Voltage Control (AVC) loop to stabilize the accelerating voltage, the ΔR loop and the phase loop to damp the synchrotron oscillation. Position and phase of the synchrotron beam is measured by an electrostatic beam monitor and fed back to the RF Controller. The phase and amplitude of the applied rf is available from a pick-up located at the rf cavity. These signals are returned to the RF Controller for feed back..

Figure 3 shows a photograph of the RF Controller. The controller has 6 outputs, 3 feedback signal inputs and 14 timing signal inputs all on the front-panel. 2 of 6 outputs are rf signals (frequency and amplitude modulated) and the other 4 are constant voltage outputs (frequency modulated only.) The constant voltage outputs are used as reference for the phase and position monitors. The 3 feed-back inputs correspond to V, ΔR and phase. Timing signals are plugged in by optical link connectors.

2.1 Data Transfer from HP-RT

The RF Controller has two 32MB DRAMs for reference data storage. The reference data are created on the control PC, which also serves as the man-machine interface for the synchrotron. Data is downloaded to the RF Controller through a HP-RT CPU in the VME crate. Because of the large size of the reference data, the rf control system is linked by Ethernet whereas the rest of the accelerator system is linked by MELSEC/NET-10.

A maximum of 1 MB of memory has been allotted to each synchrotron pattern, corresponding to 3 seconds of operation. 60 different patterns can be stored on-board, each pattern corresponding to a different extraction energy, or a different feedback gain, for instance. For our use, the typical pattern is about 600kB. This amount of data can be transferred from the PC to the RF Controller in about 2 seconds over the network at 10MB/sec. For 60 patterns the data transfer takes about 2 minutes.

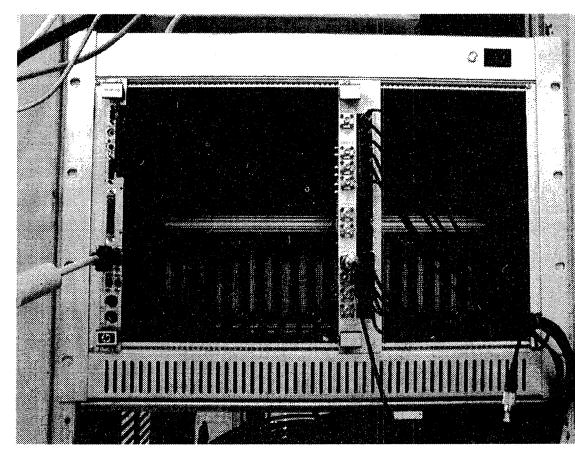

Fig.3 A photograph of RF Controller

2.2 Memory Block Structure

The pattern to be used can be selected out of the 60 available patterns from either the PC or the HP-RT. It is also possible to switch from one reference pattern to another between synchrotron cycles by sending a trigger signal to the HP-RT over Ethernet. From the PC, control commands can also be sent to the RF Controller, such as starting or stopping a pattern, and changing the feedback gain.

The 32 MB memory is divided into two groups A and B

of 30 patterns each. It is possible to download a reference data to group B(A) memory from the control PC, while a pattern in group A(B) is being used to operate the synchrotron. This feature is useful for accelerators which frequently change the extraction energy. It is also possible to write output data (the difference between reference and feedback data) into group B(A) memory and to upload the information to a PC while group A(B) is in use.

2.3 Memory Address Management

Data for a single synchrotron cycle is stored in memory in 6 separate segments: (1) injection and rf capture, (2) acceleration, (3) flat top, (4) start of deceleration, (5) deceleration, and (6) flat bottom. The timing to switch from one segment to another is event-driven, controlled by signals from the timing server. The memory clock is switched between a 50 kHz "T clock" and a 0.2 Gauss "B clock." Event signals determine when to switch between T and B clocks or to turn the feedback on/off.

Each section of patterned data is assigned a leading address. When the timing server issues an event signal, the read-out memory address jumps to the next segment. During the jump, data smoothing is executed for 10 clock cycles to avoid a discontinuity in the output signal.

2.4 Feedback and the Analog Circuit

In comparison to the DSP, FPGAs have the advantage of data processing speed. A parallel circuit can be designed specialized to a certain application. The processing time can be made very much shorter compared to the DSP which works by software. The FPGA program is stored in an EPROM, and loaded when the controller is powered up. Modification to the software can be made rather easily by rewriting the EPROM.

Data processing time for the three feedback loops need less than 10 FPGA clocks. For our controller the FPGA clock runs at 10 MHz. This can be made as high as 100 MHz but the clock rate has been matched to the D/A conversion rate of 1 MHz. A typical updating time is 1.6 μs, including the conversion time of the DDS and the DAC. The electronics is thus fast enough for a 100kHz feedback loop to damp the 5 kHz synchrotron oscillation.

Another advantage of speed is that digitization can be made sufficiently fast so that one can do away with the anti-aliasing filter at the analog input.

To test the RF Controller, we connected its output to the power amp and cavity in an open loop configuration. In a separate test, the properties of the AVC feedback loop was confirmed. Figure 4 shows the output signal of the RF Controller and the detected signal in the AVC test. The low level signal was fed back to the rf monitor directly, bypassing the power amp and cavity. A step function was used as the reference data. The result shown is with AVC feedback ON, and feedback gain parameter set at 30 which is three times the minimum gain for stability. The rise time is determined by a capacitor inserted into the Controller output.

A real-time variation of the loop gains has not been implemented in the present RF Controller. While it is not difficult to add this feature, the capability is not needed in a medical proton synchrotron.

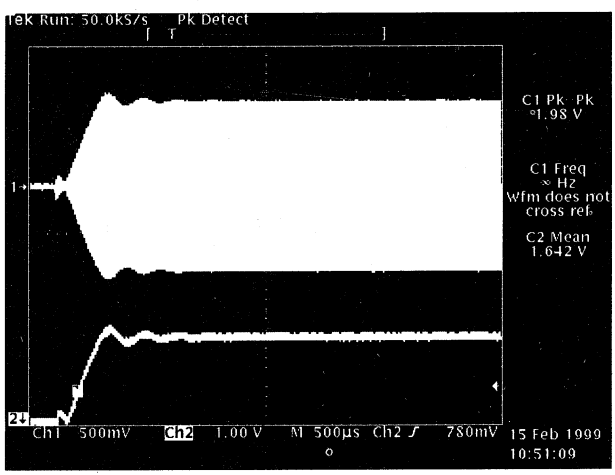

Fig.4 Output signal of the RF Controller and the detected signal in the AVC test

3 Conclusion

A low level rf control system for a proton synchrotron has been designed and built. The system is based on FPGA technology for fast processing and easy modification. We have confirmed that such a system can process all low level controls within 1.6μs. The system can be speeded up by using faster ADC/DACs. This implies the possibility of using the FPGA-based RF Controller to change the feedback parameters on line, even in a fast cycling synchrotron.

We are planning to install this RF Controller in a 250 MeV proton synchrotron under construction. The beam test will give us an opportunity to test all 3 feedback loops and to optimize the feedback parameters. At that time, software will be available for creating and modifying the patterned data from the control PC.

Acknowledgement

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