SINAP Timing System and Upgrading Schedule

Electronics Group
Beam Instrumentation & Control Division
SINAP
Dec 2010
Outline

☞ SINAP timing system structure
☞ Hardware List & Specification
☞ Performance Testing
☞ Upgrading Schedule
June 2008 prototype EVR on 1Gbps
March 2009 prototype EVG on 1Gbps
July 2009 prototype EVR & EVG on 2.5Gbps
Sep 2009 VME interface
Jan 2010 prototype Switch with data exchange function
Oct 2010 formal products released
Structure of Event Timing System
SINAP timing system structure
Hardware List

❖ SINAP timing system:

- EVG
- EVR
- FANOUT
- TTL VME Transition Board
- Plastic fiber VME Transition Board
- Multimode fiber O/E
- Plastic fiber O/E
EVG

 Specification

VME 6U module; A16D32 addressing
Input:  1ch RF clock (0 – 10 dBm)
       1ch AC line (3Vp-p typical)
Output: 1ch multi-mode fiber
        1ch Sequence RAM trigger
               (3.3V TTL)
EVG
EVR

✈️ Specification

VME 6U module; A16D32 addressing
Input: 1ch multi-mode fiber
1ch interlock input (3.3V TTL)
Output: 3ch 3.3V TTL trigger/clock
3ch 2.5V LVPECL trigger/clock
1ch CML RF recovery clock
2ch Multi-mode fiber trigger
FANOUT

重中之 Specification

VME 6U module
Input: 1ch multimode fiber
Output: 12ch multimode fiber
TTL VME Transition Board

☞ Specification

VME transition board
Output: 14ch 3.3V TTL trigger
Plastic Fiber VME Transition Board

⇒ Specification

VME transition board;
Output: 14ch optic trigger
(Agilent HFBR-1528)
Multi-mode Fiber O/E

Specification

Standalone module

Input: 1ch multi-mode fiber

1ch power supply (24V/1A)

Output: 1ch 3.3V TTL (50ohm)
Plastic Fiber O/E

❖ Specification

Standalone module
Input: 1ch multi-mode fiber
1ch power supply (24V/1A)
Output: 1ch 5V TTL
Performance Testing

穩定性

coding-decoding error

VME chassis

counter EVR EVG

RF clock AC line

fiber

EVR output EVG output

Count Panel

Count A: 726942
Count B: 726942
Runtime: 101.24 hours
Performance Testing

- Jitter

EVR TTL output

Diagram with labels and measurements for performance testing.
Performance Testing

Jitter
EVR CML output

Tek Run: 10.0GS/s  Sample

Hs StdDev 12.89ps

8 Dec 2010 11:59:55
Performance Testing

- Jitter

Multi-mode O/E output
Performance Testing

Phase Shift

Phase shift with temperature changing (35ps/℃)
Upgrading Schedule

- Concept
- System Design
- Developing Schedule
Design Philosophy:
- event system structure to realize synchronization
- reflective memory structure to realize deterministic data transfer
- dedicated data frame to realize synchronization accuracy trigger
- dedicated data frame to realize deterministic latency data transfer
- dedicated design to compensate different fiber length delay
System Design

☞ Synchronization

event system structure
System Design

Deterministic Data Transfer
reflective memory structure
System Design

Frame Format

1 byte for trigger code
1 byte for data frame

<table>
<thead>
<tr>
<th>1 byte</th>
<th>1 byte</th>
</tr>
</thead>
<tbody>
<tr>
<td>trigger</td>
<td>data frame</td>
</tr>
<tr>
<td>K28.5</td>
<td>data frame</td>
</tr>
<tr>
<td>K28.5</td>
<td>data frame</td>
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<td>K28.5</td>
<td>data frame</td>
</tr>
</tbody>
</table>

The minimum interval of trigger is 8ns (2.5Gbps).
System Design

Data Frame Format

<table>
<thead>
<tr>
<th>1 byte</th>
<th>4 byte</th>
<th>8 byte</th>
</tr>
</thead>
<tbody>
<tr>
<td>K28.3</td>
<td>address</td>
<td>data</td>
</tr>
</tbody>
</table>

4 bytes for address; 8 bytes for data; 1 byte for K28.3
The maximum data transfer rate is 76.9MB/s (2.5Gbps)
System Design

Compensation

The compensation accuracy is 8ns (in 2.5Gbps)
System Structure

Hierarchy Topology

* Switch could be cascaded
Data domain

- Switch should not generate data frame;
- EVR could generate data frame;
- Switch should accept data frame from downlink;
- Switch could configure to broadcast or not broadcast data frame from downlink to uplink;
- Switch could configure to accept or not accept data frame from uplink;
Developing Schedule

Hardware List

VME module: Switch, EVR-E, EVR-O, Interlock transition board

Standalone module (Mod-bus): Switch, EVR-E, EVR-O, EVR-I, O/E

Yokogawa FA-M3R PLC module: EVR-E

3U cPCI module: EVR-E

PXI module: EVR-E
Developing Schedule

- July 2011  prototype of upgrading system
- Nov 2011  formal products of VME module
- Dec 2011  formal products of PLC module, standalone module and cPCI/PXI module